CPU Section:
The CPU is a **68B09E** (**U209**) with up to 8 MBytes of CPU *Code Space* (**U210**). The CPU code is bank selected by the use of **U211** and each bank consists of 16 KBytes. 8 KBytes of RAM (**U212**) is available to the CPU. The RAM is battery backed and has a write protected area. Battery back up is accomplished by 3-AA Cells which have a **TEST POINT VB** to check the battery voltage status. The write protected area consists of 512 Bytes used for storing game settings. This section of **RAM** can only be written to when the coin door is open. The Coin Door switch comes into the CPU on **CN6-12** and is fed into the address decoding **PAL U213**. When this memory protect signal is low writes to the protected **RAM** area are prohibited. Address decoding for the system is accomplished by one **PAL U213** and one 1-of-8 decoder **U214**.

A watchdog is used to monitor the CPU and the 5v supply. If the 5v supply is below 4.75 the watchdog will hold the CPU/Sound Board & I/O Board in reset. The watchdog must be fed at a rate of ***250ms*** or faster. The signal used to feed the watchdog comes from the EPROM Bank select signal used to load **U211**. The CPU has a timer interrupt used as a heartbeat for the system this signal comes from counter **U2**. The clock for this counter is the **CPU Q CLOCK**. Clearing the timer interrupt is done by reading the ***DIP Switch***. The timer interrupt can be observed at **TEST POINT FIRQ**. In normal operation **"FIRQ"** should be toggling at a rate of *976Hz*.

The I/O Interface **CN1** is buffered by two (2) **HC245** Chips. The CPU's reset line is buffered by **Q10** and fed over to the I/O through **CN1**. An I/O strobe signal is feed through **CN1-15** and is used to notify the I/O that a valid address is being sent.

Switches:
The Switch Matrix consists of eight (8) **2N3904** Transistors which pull one of 8 strobes 'low' to *activate* a Single Column of switches. The *Switch Return Signals* are fed into **CN7** [SWITCH ROWS] and are highly filtered and compared to a 2.5v *reference voltage*. The *Switch Return Voltage* must be below 2.5v to make a *Valid Switch Closure*. If *false switches* are appearing, check that none of the **2N3904** Transistors are permanently pulling the *strobe line low*. Only one strobe from **CN5** [SWITCH COLUMNS] should be *low at any time*. **CN6** [DEDICATED SWITCH IN] is a *Dedicated Bank of Input Switches*. Switches connected to **CN6** are connected to ground instead of a strobe and may be read at any time.

Plasma Interface:
The data path for communication to and from the Plasma Controller Board is 8 bits wide. There are separate *Input* and *Output Busses*. The *Input Bus* from the Plasma Controller to the CPU/Sound Board comes in on **CN8** [PLASMA CONTROL]-**Pins 3-10** and is fed into **U200** for input to the CPU's *Data Bus*. Data going out to the controller comes from the CPU's *Data Bus* through **U201** and onto **CN8-Pins 11-18**. Status back from the Plasma Controller comes in on **CN8-Pins 22-26** and is fed into **U202** for input to the CPU's *Data Bus*. Two control signals that go out to the Plasma Controller are **PRES** [PLASMA RESET] and **CN8-Pin 19** [**PSTB** - *Plasma Strobe*]. The Plasma Reset is software controllable through **U216/B** and also has a test point "Plasma Reset". The *Plasma Strobe Signal* to the controller is generated from **U216/A** and is *used to latch data* into the Plasma Controller.

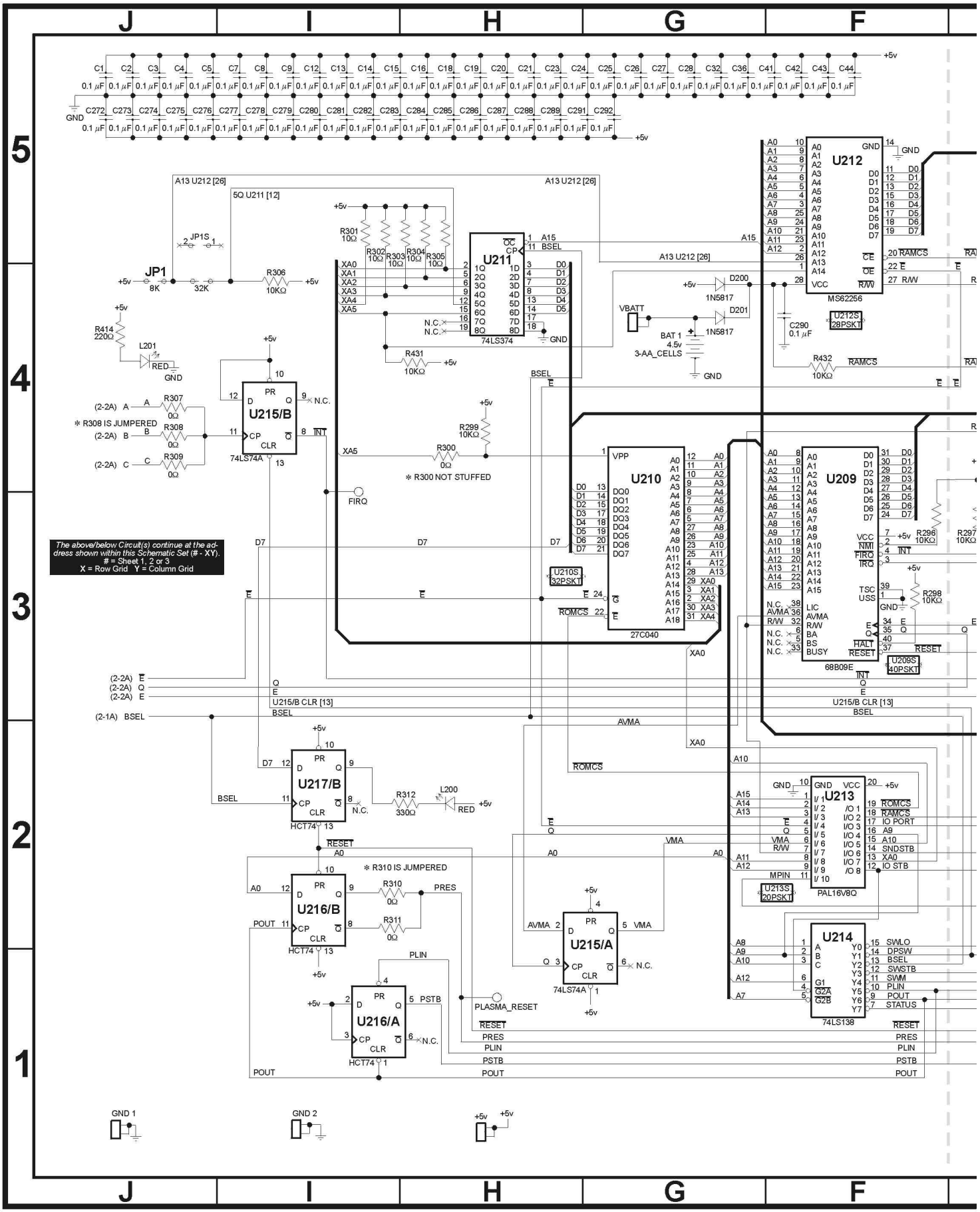
Sound Section:
The audio section consists of a **BSMT SOUND CHIP U9** Sound (Voice) EPROMs (**U17 U21 U36 U37**) **68B09E U6** and Sound Code **EPROM U7**. The **BSMT** latches sound EPROM addresses in **U13** & **U12** for output to the Sound EPROMs. Sound Data from the EPROMs is read through **U19** to the **BSMT**. The EPROMs are bank selected by **U22**. When the **BSMT** has sound data to be played out to the speakers it loads 16 bits into a 16 bit shift register made up of **U24** & **U23**. The data stream from the shift register is serially shifted into a stereo 16 bit *Digital to Analog Converter* (**DAC**). When the system is operating properly the ws (word select) input of the **DAC** will be toggling. The ws input is used to latch the right and left channel sound data into the **DAC**. If the ws line is not oscillating no analog signal will come out of the **DAC**. The **DAC** outputs are a controlled current source. These outputs are converted to a voltage by an operational amplifier **U30** to form the analog signal. **TEST POINTS AOR** and **AOL** are the outputs of the operational amplifier. These outputs are then fed directly into three power amplifiers (**TDA2030A**) or optionally into an analog volume control chip **U35** for a potentiometer volume control. The analog section has its own +5v & -5v derived from **VR1** & **VR2**. These separate supply voltages are for the **DAC U26** Operational Amplifier **U30** and analog volume control **U35**.

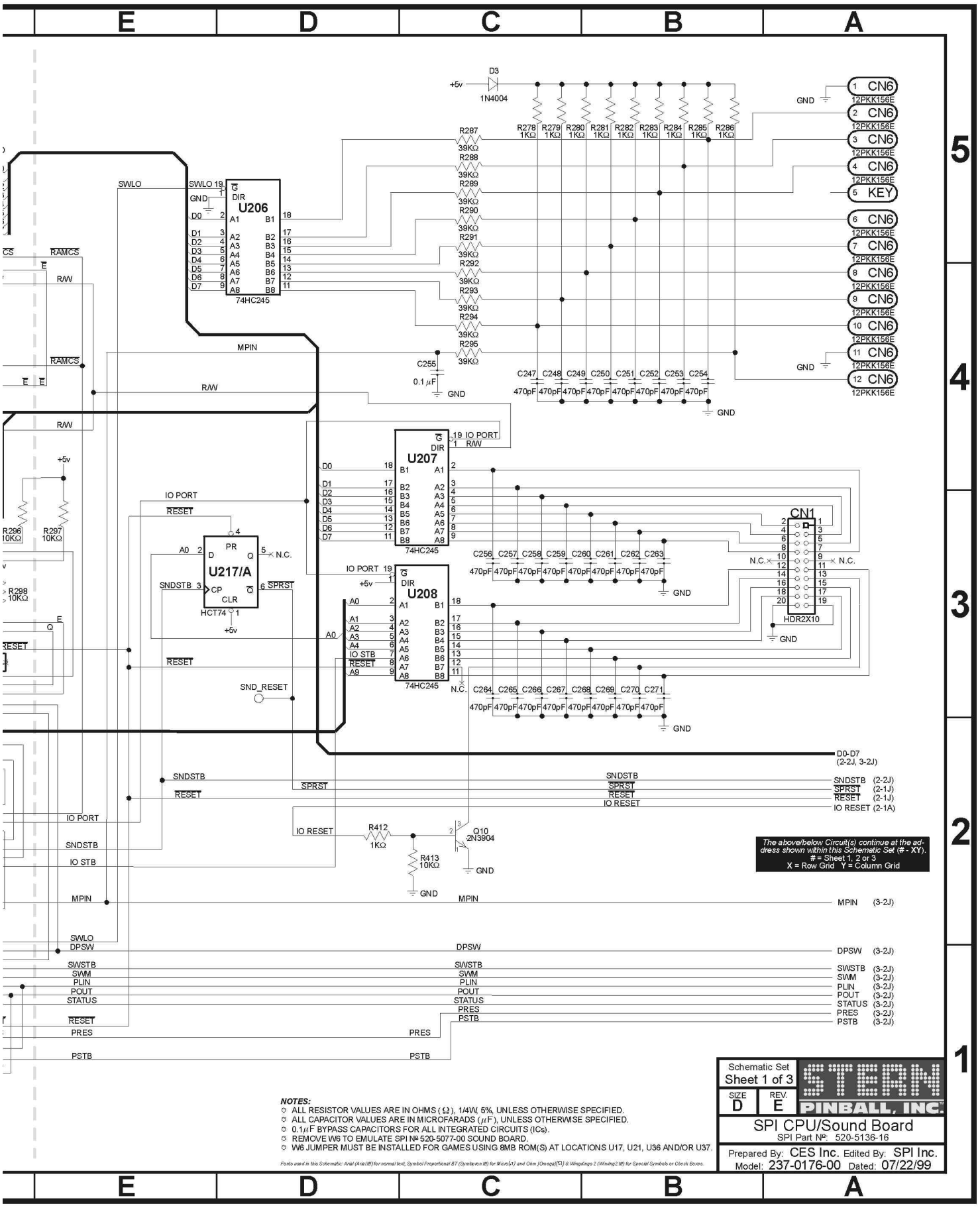
Sound calls are made from the **CPU's 68B09E U200** to the sound section by latching data into **U5**. The sound section's **CPU 68BO9E (U6)** reads in this data and handles the interfacing to the **BSMT**.

Other Test Points:
E & **Q** - The CPU signals for both **68B09E** processors. Should be at 2Mhz with **Q** leading **E** by ***500 nsec***.
24Mhz - The oscillator used for the **BSMT** & derivation of **E** & **Q**.
SND-FIRQ - The sound sections CPU interupt.
6Mhz - This clock is generated internally on the **BSMT** and is used for shifting the data samples into th **DAC**.

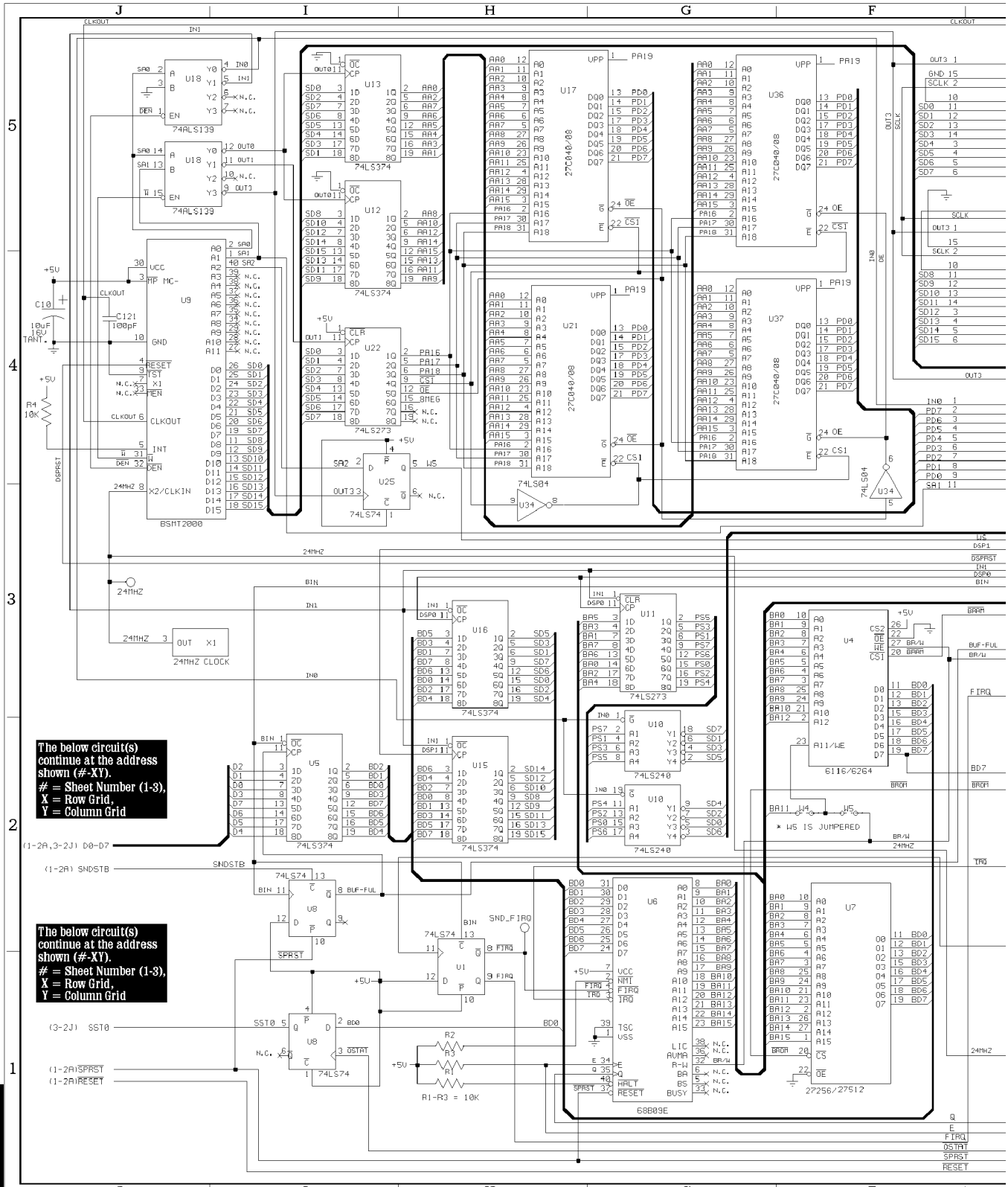
W6 Jumper - This jumper must be installed for games that use **8MB** Sound EPROMs (**U17 U21 U36 U37**). For games which use **4MB** Sound EPROMs this jumper is not installed but will operate on boards with W6 installed.

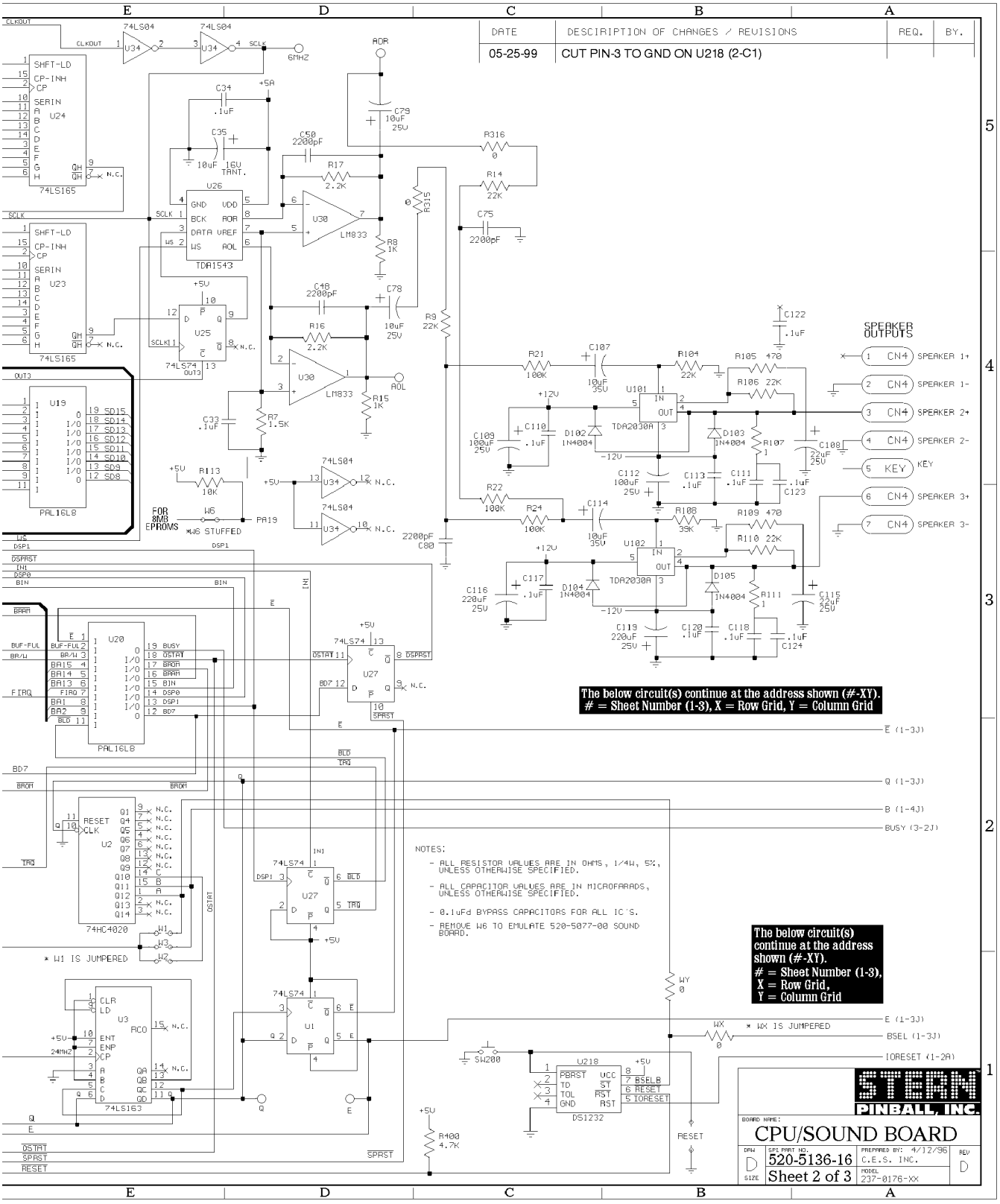
Section 5, Chapter 4: Printed Circuit Boards (PCBs)

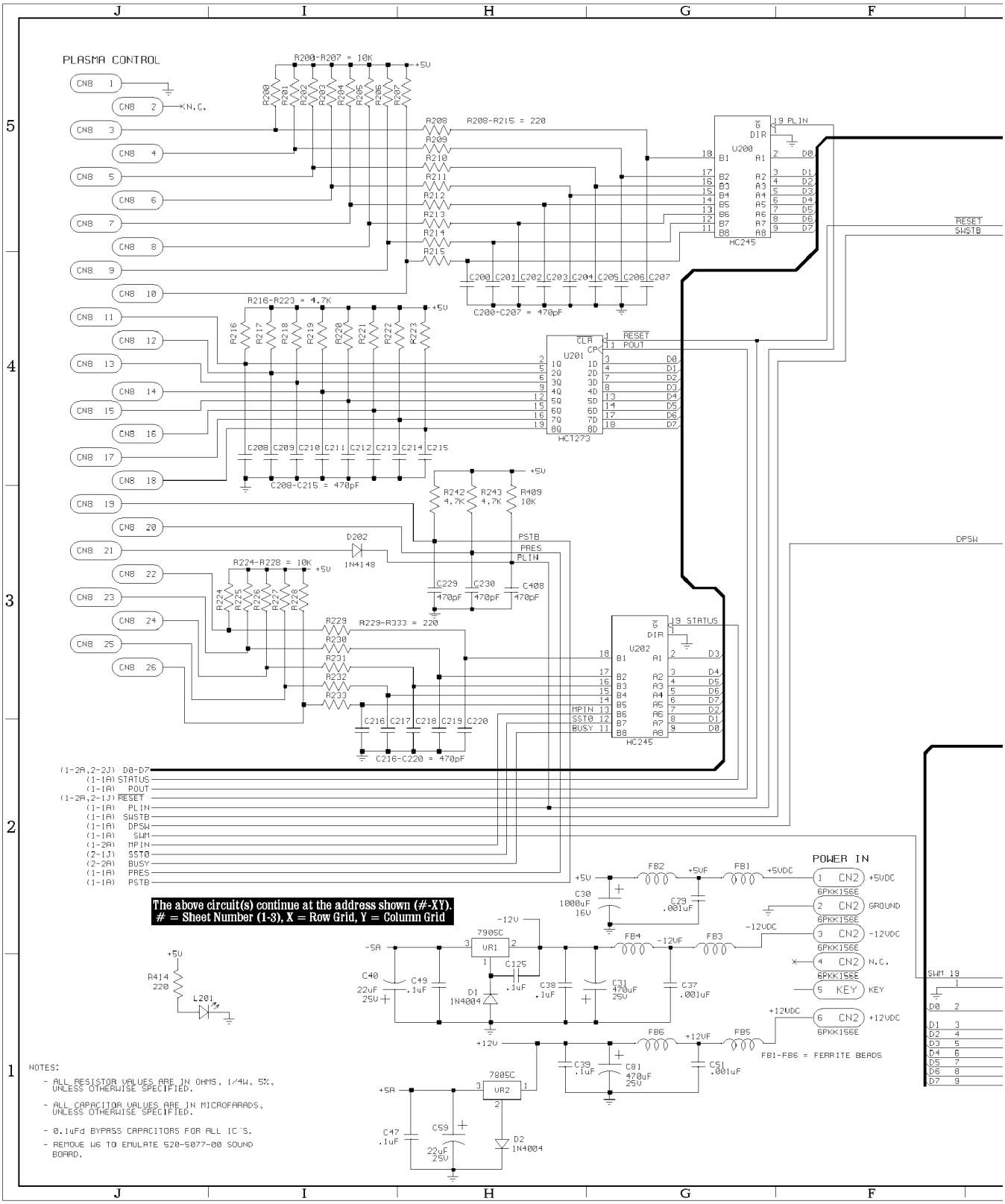

J
I
H
G
F
5
4
3
2
1
U210
27C040
U209
68B09E
U212
MS62256
U211
74LS374
U215/B
74LS74A
U217/B
HCT74
U216/B
U216/A
U215/A
U213
PAL16V8Q
U214
74LS138
JP1
JP1S
R306
10KΩ
R307
R308
R309
R310
R311
R312
330Ω
R414
220Ω
L201
RED
L200
RED
R431
10KΩ
R432
10KΩ
R296
10KΩ
R297
10KΩ
R298
10KΩ
R299
10KΩ
R300
0Ω
* R300 NOT STUFFED
* R308 IS JUMPERED
* R310 IS JUMPERED
D200
1N5817
D201
1N5817
BAT 1
4.5v
3-AA_CELLS
VBATT
C290
0.1 μF
U212S
28PSKT
U210S
32PSKT
U209S
40PSKT
U213S
20PSKT
FIRQ
PLASMA_RESET
The above/below Circuit(s) continue at the address shown within this Schematic Set (# - XY).
# = Sheet 1, 2 or 3
X = Row Grid Y = Column Grid
GND 1
GND 2

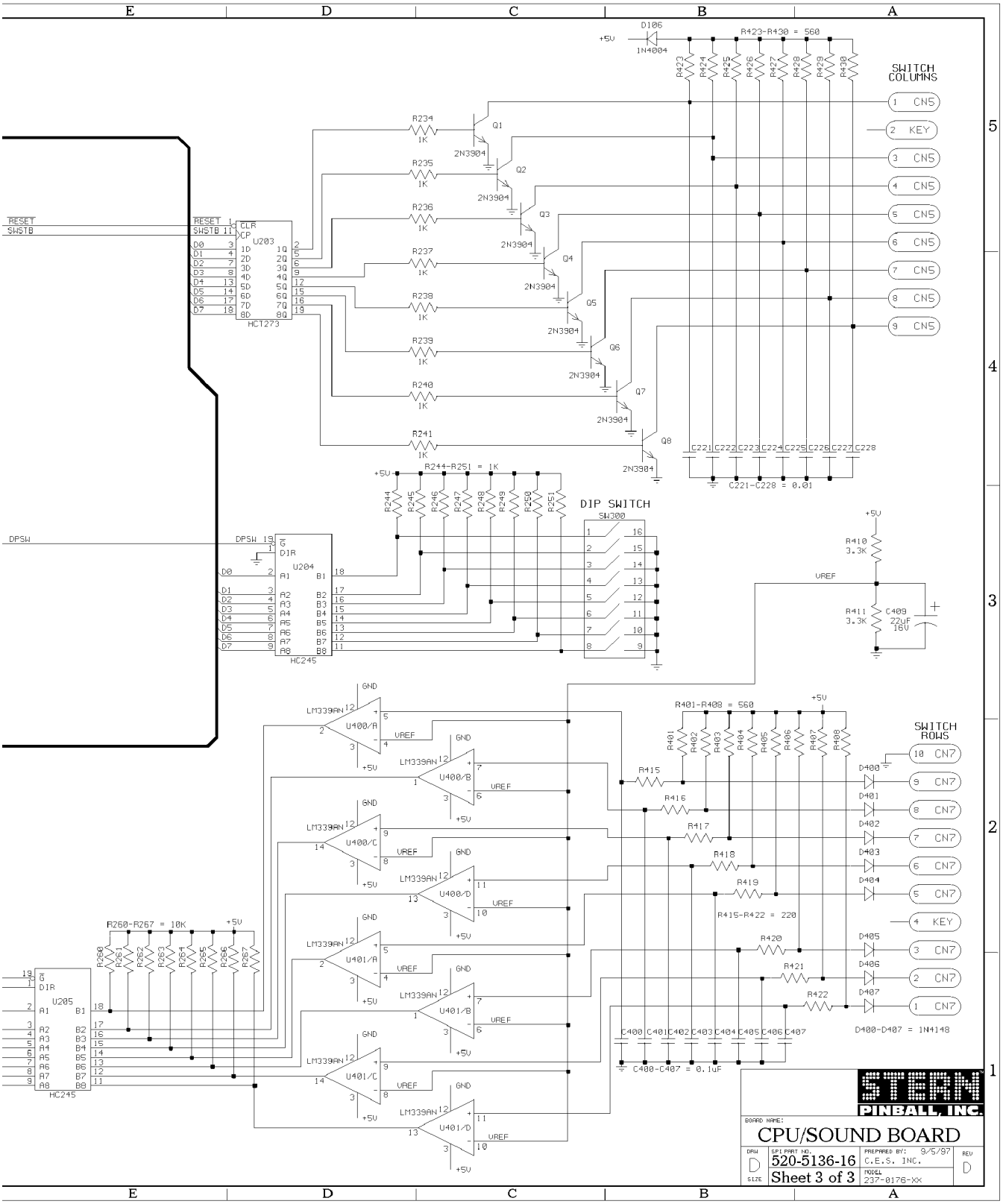

E
D
C
B
A
5
4
3
2
1
U206
74HC245
U207
74HC245
U208
74HC245
U217/A
HCT74
CN1
HDR2X10
D3
1N4004
+5v
GND
SWLO
RAMCS
R/W
MPIN
IO PORT
RESET
SNDSTB
SPRST
IO RESET
SND_RESET
D0-D7
(2-2J, 3-2J)
SNDSTB (2-2J)
SPRST (2-1J)
RESET (2-1J)
IO RESET (2-1A)
MPIN (3-2J)
DPSW (3-2J)
SWSTB (3-2J)
SWM (3-2J)
PLIN (3-2J)
POUT (3-2J)
STATUS (3-2J)
PRES (3-2J)
PSTB (3-2J)
IO STB
DPSW
SWSTB
SWM
PLIN
POUT
STATUS
PRES
PSTB
R412
1KΩ
Q10
2N3904
R413
10KΩ
The above/below Circuit(s) continue at the address shown within this Schematic Set (# - XY).
# = Sheet 1, 2 or 3
X = Row Grid Y = Column Grid
Schematic Set
Sheet 1 of 3
SIZE
D
REV.
E
STERN
PINBALL, INC.
SPI CPU/Sound Board
SPI Part №: 520-5136-16
Prepared By: CES Inc. Edited By: SPI Inc.
Model: 237-0176-00 Dated: 07/22/99
NOTES:
ALL RESISTOR VALUES ARE IN OHMS (Ω), 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.
ALL CAPACITOR VALUES ARE IN MICROFARADS (μF), UNLESS OTHERWISE SPECIFIED.
0.1μF BYPASS CAPACITORS FOR ALL INTEGRATED CIRCUITS (ICs).
REMOVE W6 TO EMULATE SPI № 520-5077-00 SOUND BOARD.
W6 JUMPER MUST BE INSTALLED FOR GAMES USING 8MB ROM(S) AT LOCATIONS U17, U21, U36 AND/OR U37.

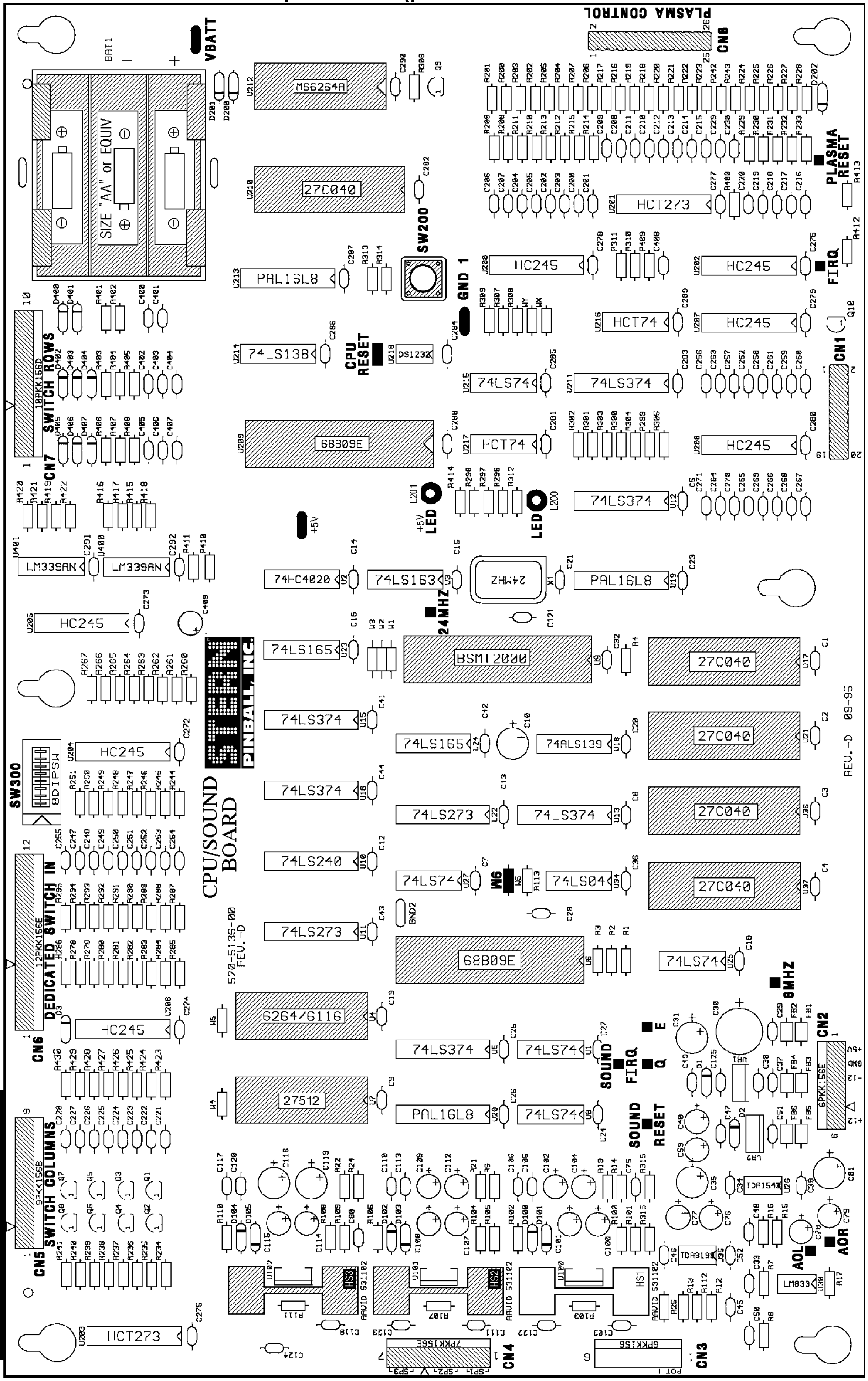
CPU/Sound Board Schematic (Sheet 2 of 3)




DATE
DESCIRIPTION OF CHANGES / REVISIONS
REQ.
BY.
05-25-99
CUT PIN-3 TO GND ON U218 (2-C1)
SPEAKER OUTPUTS
CN4 SPEAKER 1+
CN4 SPEAKER 1-
CN4 SPEAKER 2+
CN4 SPEAKER 2-
KEY KEY
CN4 SPEAKER 3+
CN4 SPEAKER 3-
The below circuit(s) continue at the address shown (#-XY).
= Sheet Number (1-3), X = Row Grid, Y = Column Grid
NOTES:
- ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.
- ALL CAPACITOR VALUES ARE IN MICROFARRADS, UNLESS OTHERWISE SPECIFIED.
- 0.1uFd BYPASS CAPACITORS FOR ALL IC'S.
- REMOVE W6 TO EMULATE 520-5077-00 SOUND BOARD.
* W1 IS JUMPERED
* WX IS JUMPERED
BOARD NAME:
CPU/SOUND BOARD
SPI PART NO.
520-5136-16
Sheet 2 of 3
PREPARED BY: C.E.S. INC.
4/12/96
MODEL
237-0176-XX
DRW SIZE D
REV D
STERN PINBALL, INC.


PLASMA CONTROL
R200-R207 = 10K
+5U
CN8 1
CN8 2
N.C.
CN8 3
CN8 4
CN8 5
CN8 6
CN8 7
CN8 8
CN8 9
CN8 10
CN8 11
CN8 12
CN8 13
CN8 14
CN8 15
CN8 16
CN8 17
CN8 18
CN8 19
CN8 20
CN8 21
CN8 22
CN8 23
CN8 24
CN8 25
CN8 26
R208 R208-R215 = 220
R209
R210
R211
R212
R213
R214
R215
C200 C201 C202 C203 C204 C205 C206 C207
C200-C207 = 470pF
U200
DIR
19 PLIN
HC245
RESET
SWSTB
R216-R223 = 4.7K
U201
CLR
CP
RESET
POUT
HCT273
C208 C209 C210 C211 C212 C213 C214 C215
C208-C215 = 470pF
R242 4.7K
R243 4.7K
R409 10K
D202
1N4148
PSTB
PRES
PLIN
R224-R228 = 10K
C229 C230 C408
470pF
DPSW
R229 R229-R333 = 220
R230
R231
R232
R233
U202
19 STATUS
HC245
C216 C217 C218 C219 C220
C216-C220 = 470pF
(1-2A,2-2J) D0-D7
(1-1A) STATUS
(1-1A) POUT
(1-2A,2-1J) RESET
(1-1A) PLIN
(1-1A) SWSTB
(1-1A) DPSW
(1-1A) SWM
(1-2A) MPIN
(2-1J) SST0
(2-2A) BUSY
(1-1A) PRES
(1-1A) PSTB
The above circuit(s) continue at the address shown (#-XY).
= Sheet Number (1-3), X = Row Grid, Y = Column Grid
POWER IN
FB2 +5VF
FB1 +5VDC
C30 1000uF 16V
C29 .001uF
CN2 6PKK156E
+5VDC
GROUND
-12VDC
N.C.
KEY
+12VDC
SWM 19
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
-12V
7905C
VR1
C125 .1uF
C40 22uF 25V
C49 .1uF
D1 1N4004
C38 .1uF
C31 470uF 25V
C37 .001uF
FB4 -12VF
FB3
+12V
FB6 +12VF
FB5
C39 .1uF
C81 470uF 25V
C51 .001uF
FB1-FB6 = FERRITE BEADS
7805C
VR2
C47 .1uF
C59 22uF 25V
D2 1N4004
R414 220
L201
NOTES:
- ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.
- ALL CAPACITOR VALUES ARE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
- 0.1uFd BYPASS CAPACITORS FOR ALL IC'S.
- REMOVE W6 TO EMULATE 520-5077-00 SOUND BOARD.


SWITCH COLUMNS
SWITCH ROWS
DIP SWITCH
SW300
R423-R430 = 560
R244-R251 = 1K
R401-R408 = 560
R415-R422 = 220
R260-R267 = 10K
C221-C228 = 0.01
C400-C407 = 0.1uF
D400-D407 = 1N4148
U203
U204
U205
HCT273
HC245
LM339AN
2N3904
1N4004
STERN PINBALL, INC.
BOARD NAME:
CPU/SOUND BOARD
520-5136-16
Sheet 3 of 3
C.E.S. INC.
3/5/97
237-0176-XX



TEST POINTS:

- << VBATT
- << PLASMA RESET
- << FIRQ
- << SW200
- << GROUND 1
- << CPU RESET
- << L201 LED+5v
- << L200 LED
- << +5v
- << 24 Mhz
- << W6 requires a Jumper if using 8MB EPROMs in U17, U21, U36 and/or U37
- << 6 Mhz
- << E
- << SOUND FIRQ
- << Q
- << SOUND RESET
- << AOR
- << AOL

CPU/Sound Board Parts

ITEM	QTY	PART NUMBER	REF-DESIGNATOR	DESCRIPTION (NS = Not Stuffed)
—	**1**	**520-5136-16**	**CPU/Sound Board Mono (FCC FEB98)**	**Complete PCB Assembly**
1	1	124-5001-00	VR2	LM7805CT +5v Regulator
2	5	121-5051-00	R12, R13, R19, R21, R22, R24	100K Ω 1/4W Res. (R19: NS)
3	2	121-5009-00	R103, R107, R111	1K Ω 1/4W Res. (R103: NS)
4	38	121-5011-00	R1>R4, R113, R200>R207, R224>R228, R244>R251, R260>R267, R296>R299, R301>R306, R409, R413	10K Ω 1/4W Res. (R200>R207, R409, R413: NS)
5	5	121-5023-00	R9, R14, R100, R102, R104, R106, R110	22K Ω 1/4W Res. (R100, R102: NS)
6	20	121-5009-00	R15, R8, R234>R241, R278>R286, R412	1K Ω 1/4W Res.
7	4	121-5043-00	R16, R17, R25, R112	2.2K Ω 1/4W Res.
8	1	121-5018-00	R7	1.5K Ω 1/4W Res.
9	2	121-5046-00	R101, R105, R109	470K Ω 1/4W Res. (R101: NS)
10	9	121-5045-00	R108, R287>R294	39K Ω Res.
11	1	121-5036-00	R312	330 Ω 1/4W Res.
12	12	n/a	R300, R308>R311, R313>R316, WX, WY	0Ω *Jumper Wire (24ga.)*
13	15	121-5033-00	R208>R215, R229>R233, R414>R422	220 Ω 1/4W Res. (R208>R215: NS)
14	11	121-5021-00	R216>R223, R242, R243, R400	4.7K Ω 1/4W Res.
15	16	121-5047-00	R401>R408, R423>R430	560 Ω 1/4W Res.
16	2	121-5048-00	R410, R411	3.3K Ω 1/4W Res.
17	1	100-0049-00	U3	74LS163
18	1	(See Pg. **DR. ❸** Table)	U7	27512 EPROM
19	1	045-5015-07	CN4	7PKK156 (PIN5=KEY)
20	1	Not Used	RESET	*Do Not Stuff*
21	5	(See Pg. **DR. ❸** Table)	U17, U21, U36, U37, U210	27C040 EPROM
22	2	100-5008-00	U23, U24	74LS165
23	4	125-5017-00	C76>C79	10uF, 25v, Radial Lytic Cap.
24	4	125-5020-00	C40, C59, C101, C108, C115	22uF, 25v, Radial Lytic Cap. (C101: NS)
25	2	125-5017-00	C100, C10,7 C114	10uF, 35v, Radial Lytic Cap. (C100: NS)
26	2	125-5015-00	C102, C104, C109, C112	100uF, 25v, Rad. Ltc. Cap. (C102, C104: NS)
27	1	125-5014-00	C409	22uF, 16v, Radial Lytic Cap.
28	1	100-5016-00	U35	TDA1899
29	1	125-5037-00	C30	1000uF, 16v, Radial Lytic Cap.
30	1	100-0027-00	U34	74LS04
31	1	100-0043-00	U18	74ALS139
32	6	100-0064-00	U5, U12, U13, U15, U16, U211	74LS374
33	1	100-0249-00	U2	74HC4020
34	1	100-0149-00	U10	74LS240
35	6	n/a	W1>**W6** (Jumper required @ W6 if using 8MB EPROMs)	0Ω *Jumper Wire (24ga.)*
36	2	125-5019-00	C31, C81	470uF, 25v, Radial Lytic Cap.
37	2	125-5017-00	C10, C35	10uF, 16v, Radial Tant. Cap.
38	2	125-5012-00	C116, C119	220uF, 25v, Radial Lytic Cap.
39	1	045-5015-06	CN2	6PKK156 (PIN 5=KEY)
40	1	140-0011-00	X1	24Mhz
41	1	105-0116-00	U9	BSMT2000
42a	1	965-0136-00	**U19 - YELLOW DOT**	PAL16L8 (Programmed) - **YELLOW DOT**
42b	1	965-0137-00	**U20 - WHITE DOT**	PAL16L8 (Programmed) - **WHITE DOT**
42c	1	965-6504-00	**U213- BLUE DOT**	PAL16L8 (Programmed) - **BLUE DOT**
43	5	100-0037-00	U1, U8, U25, U27, U215	74LS74
44	3	125-5043-00	C29, C37, C51	0.001uF, (102), Cap.
45	79	125-5031-00	C1>C5, C7>C9, C12>C16, C18>C21, C23>C26, C28, C32>C34, C36, C38, C39, C41>C47, C49, C52, C102 C103, C105, C106, C110, C111, C113, C117, C118, C120, C122>C125, C255, C272>C292, C400>C407	0.1uF, (104), Axial Cer. Cap. (C102, C103, C105, C106: NS)
46	1	125-5038-00	C121	100pF, (101), Cap.
47	4	125-5039-00	C48, C50, C75, C80	0.0022uF, (222), Cap.
48	39	125-5028-00	C200>C220, C229, C230, C247>C254, C256>C271	470pF, (471), Cer. Cap. (C200>C207: NS)
49	8	125-5029-00	C221>C228, C408	0.01uF, (103), 100v Cap. (C408: NS)
50	1	045-5015-06	CN3	6PKK156
51	1	100-0375-00	U30	LM833
52	2	100-0022-00	U22 U11	74LS273
53	7	112-5003-00	D1>D3, D100>D105	1N4004, Diode (D100, D101: NS)
54	2	112-5008-00	D200, D201	1N5817, Diode
55	8	112-0054-00	D202, D400>D407	1N4148, Diode (D202: NS)
56	1	124-5002-00	VR1	LM7905CT -5v Regulator
57	2	100-5016-20	U100>U102	TDA2030V (U100: NS)
58	1	100-5018-00	U26	TDA1543
59	1	n/a	SW200	B3F4000
60	1	165-5099-00	**L200**	**LED T1-3/4 DIFFUSER LED**
61	1	165-5099-00	**L201**	**LED T1-3/4 DIFFUSER LED**
62	2	100-5015-00	U216, U217	HCT74
63	1	100-0148-00	U214	74LS138
64	1	105-0046-00	U212	MS6264A
65	1	100-0189-01	U6, U209	68B09E
66	1	545-5685-00	BAT1 BATTERY HOLDER	3-AA CELLS 4.5v
67	1	045-5015-01	CN1	20-Pin, 0.1 HEADER
68	10	n/a	6MHZ AOR Q AOL 24MHZ	*Test Points* - NS
69	10	110-0069-00	Q1>Q10	2N3904, Transistor
70	1	045-5013-00	CN5	9PKK156 (PIN 2=KEY)
71	2	100-5012-00	U201, U203	74HCT273
72	6	100-0338-00	U200, U202, U204>U208	74HC245 (U200: NS)
73	1	100-5023-00	U218	DS1232
74	1	045-5015-26	CN8	26-Pin, 0.1 HEADER
75	1	045-5014-01	CN7	10PKK156 (PIN 4=KEY)
76	4	n/a	VBATT +5v GND1, GND2	*Test Point Wire (24ga.) Loops*
77	1	045-5015-00	CN6	12PKK156 (PIN 5=KEY)
78	1	181-5002-00	SW300	8-Pin, Dip Switch
79	2	100-0377-00	U400, U401	LM339AN
80	1	105-0052-05	U4	6116 RAM
81	3	535-5000-10	U100>U102	AAVID 531102
82	3	077-5209-00	U6, U9, U209	40-Pin, IC Socket
83	5	077-5217-00	U17, U21, U36, U37, U210	32-Pin, IC Socket
84	3	077-5208-00	U4, U7, U212	28-Pin, IC Dip Socket
85	1	n/a	U1 (@ Pins 5 & 6)	100pF, Cap.