LUNAR LANDER

SIGNATURE ANALYSIS

GUIDE

Introduction

This guide is intended as an aid to troubleshooting the Lunar Lander video game PCB. The Signature Analyzer used to produce this guide was an HP5004a. If it is found that the signatures hold up for other makes/models of Signature Analyzers then please let me know and I can add some kind of compatibility list to the document.

To get the most out of the guide you'll need

Signature Analyzer (HP5004a)
Schematics for Lunar Lander
6502 NOP card (See the separate document 6502NOP for instructions on how to build your own NOP card)
IC Clips
Some jumper wires (3 or 4 should be sufficient)

The scope of the guide is limited in that it will not enable you to fault find the entire PCB. It should, however, be good for the following sections of the PCB:

Address Bus Buffers, Address Decoding Circuitry, Clock Circuit, Program ROMs and Data Buffer, Vector Generator Address Selector, Vector Generator RAM Select, Vector Generator ROMs and the Vector Generator Data Buffer.

The Clock Circuit test is very limited. The reason being is that I much prefer to check the clock chain with a scope. If you want to figure out the signatures for the Clock Circuit then pass on the information and I'll include it in the document. If you want a detailed description of these sections (and more) please refer to the Lunar Lander schematic / drawing package.

Using The Guide

For those of you who have used Atari Signature Analysis guides before then this should look familiar and there's probably no need to read through this section. For the rest of you, here's a quick run down. Every section should start with the settings for the Analyzer, something like this

A. SA Settings for xxxxx Test

Probe	Trigger	IC Pin	Test Pt.
Start	+ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	$\phi 2$

The probe column refers to either the Start, Stop or Clock probes from the Signature Analyzer.

The trigger column sets up the Start/Stop/Clock buttons on the front of the Analyzer. I have used –ve to indicate the negative going edge of the pulse (or the falling edge).
I have used +ve to indicate the positive going edge of the pulse (or the rising edge).
The IC Pin column refers to the point where the appropriate probe should be attached.
The Test Pt. column refers to an equivalent Test Point on the boards where the probe may be attached.

For example, in the example above the Start probe should be connected to pin 25 of IC C2. The Start button on the front of the Analyzer should be in the fully out position to indicate a positive going edge. Similarly, the Stop probe should be connected to the same IC/Pin as the Start probe but the Stop button on the Analyzer should be pressed in to indicate a negative going edge.

The section immediately following the set up procedure contains the signatures for that part of the test. The same structure for the Set Up was employed as explained below.

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
C1-20	+5V	0003
C1-9	AB0	UUUU
C1-12	AB1	FFFF

Here, with the Analyzer probe on pin 20 of IC C1 you should get a reading of 0003. On pin 9 of IC C1 you should get a reading of UUUU. And so on.

A signature denoted by an (*) indicates that signature may be unstable. Try taking the signature with a 1Kohm resistor connected between the probe tip and +5V.

Down To Business

One of the things I like about this testing method is that you don't need to have the PCB in the cabinet. If you prefer to work in the back of the cabinet then that's fine. If you have a bench/test area with a +5V PSU (as I'm sure most of you have), then you can sit comfortably at the bench. Simply connect Ground (pins 1 and 22 on the edge connector) and +5V (pins 2 and 21 on the edge connector) to the PCB, remove the game MPU and replace it with your NOP card and you're ready to start.

Just set up the Analyzer as indicated and start probing for those signatures. Always remember to have the Watchdog disabled as this will lead to permanently unstable signatures.

What To Do When You Find An Incorrect Signature

If you find a signature that doesn't match the guide, check your set up first. If your set up is OK then you'll need to trace the fault. Rather than having a long winded ramble from me it would be better to look at the following link on Al Kossow's page. If you haven't already had a look at his site then I'd definitely recommend having a look as it's a bit of a gold mine.

http://www.spies.com/arcade/TE/SigAnalNotes.pdf

After you've had a look through the document then you should know enough to start tracing the fault. It should also give you a bit more information on Signature Analysis in general.

Some Common Faults

The two most common faults I've come across are bad sockets and shorted traces. During the Signature Analysis the bad socket problem is highlighted by the fact that the signatures are unstable. You may get some stable and some not. When you get unstable signatures whilst doing the ROM tests it does not necessarily indicate a bad ROM. Reseating the ROM or replacing the socket is usually a good place to start. The problem of shorted traces is usually down to something being dragged across the board. Sometimes they can be quite hard to see but Signature Analysis shows it up quite good.

Disclaimer

If you toast yourself, your house, your dog, your family or more importantly your video game, then it's not my fault. You use the information contained in this guide at your own risk. Good luck.

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** Tie the Watchdog Disable test point to ground **

1. Address Lines

A. SA Settings for Address Buffer Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
C2-20	+5V	0003
C2-7	AB0	UUUU
C2-12	AB1	FFFF
C2-9	AB2	8484
C2-14	AB3	P763
C2-5	AB4	1U5P
C2-16	AB5	0356
C2-18	AB6	U759
C2-3	AB7	6F9A
B2-14	AB8	7791
B2-16	AB9	6321
B2-12	AB10	37C5
B2-7	AB11	6U28
B2-9	AB12	4FCA
C3-23	A13	4868
C3-24	A14	9UP1

2. Address Decoding

A. SA Settings for Address Decoder Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
E4-4	SINP0	AF76
E4-5	SINP1	6913
E4-6	OPTS	13HP
E4-7	POTIN	PCCA
E4-9	PMEM	3282
E4-10	VMEM	AH63
E4-11	I/O	7APA
E4-12	ZPAGE	P508
L3-4	PROM0	P933
L3-5	PROM1	UH4P
L3-6	PROM2	A04H
L3-7	PROM3	86C1
D6-10		3H01
C6-8		3H02

C. SA Settings for Address Decoder Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C4-3	6MHz

** Tie R/W test point to ground **

D. Signatures

Logic Probe On IC	Signal Name	Signature

D6-14	+5V	00UP
D6-4		0066 **(*)**
E5-8		7U7C

L6-1	DMAGO	383U
L6-2	OUTCK	P759
L6-3	WDCLR	90P8
L6-5	DMACNT	A43F
L6-7	AUDIO	81F6
L6-9	NOISERESET	1A35

** Remove jumper from R/W test point **

3..Watchdog Circuit

A. SA Settings for Watchdog Circuit Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

** Tie L6-12 to ground **

B. Signatures

Logic Probe On IC	Signal Name	Signature
C6-14	+5V	0003
C6-6		752C
D5-6		HH52
D5-8		0000

** Remove jumper from L6-12 **

NOTE : I have my doubts about the signature at D5-6. Need to confirm.

4..Clock Circuit

A. SA Settings for Clock Circuit Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
B4-6		763H
B4-8	3KHz	8A4U
B4-9	6KHz	3C2U
B4-10	12KHz	9720

5 ROM And Data Lines

A. SA Settings for ROM0 Test (F1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-4	
Stop	+ve	L3-4	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	-01 ROM Signature	-02ROM Signature
F1-24	+5V	0003	0003
F1-9	DB0	2831	FF08
F1-10	DB1	2U07	PF63
F1-11	DB2	F813	A3FF
F1-13	DB3	C2A6	C2CF
F1-14	DB4	16PP	03C7
F1-15	DB5	FP73	4386
F1-16	DB6	431C	FC9C
F1-17	DB7	967C	6CFP

C. SA Settings for ROM1 Test (D/E1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-5	
Stop	+ve	L3-5	
Clock	-ve	C3-39	ϕ2

D. Signatures

Logic Probe On IC	Signal Name	-01 ROM Signature	-02ROM Signature
D/E1-9	DB0	52H5	75U9
D/E1-10	DB1	2H01	H931
D/E1-11	DB2	PPF5	6F09
D/E1-13	DB3	1P8P	688U
D/E1-14	DB4	4C5P	U4AF
D/E1-15	DB5	4F43	6H05
D/E1-16	DB6	6U3A	9363
D/E1-17	DB7	49U7	5H00

E. SA Settings for ROM2 Test (C1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-6	
Stop	+ve	L3-6	
Clock	-ve	C3-39	ϕ2

F. Signatures

Logic Probe On IC	Signal Name	-01 ROM Signature	-02ROM Signature
C1-9	DB0	PA6P	PA6P
C1-10	DB1	F26P	F26P
C1-11	DB2	PH7F	PH7F
C1-13	DB3	C8U6	C8U6
C1-14	DB4	56A3	56A3
C1-15	DB5	6H51	6H51
C1-16	DB6	4H77	4H77
C1-17	DB7	211U	211U

G. SA Settings for ROM3 Test (B1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-7	
Stop	+ve	L3-7	
Clock	-ve	C3-39	ϕ2

H. Signatures

Logic Probe On IC	Signal Name	-01 ROM Signature	-02ROM Signature
F1-9	DB0	FC72	0P4H
F1-10	DB1	FH21	1F5F
F1-11	DB2	7A0H	37UU
F1-13	DB3	UF65	U985
F1-14	DB4	1PF4	758C
F1-15	DB5	93FU	7U6C
F1-16	DB6	6H72	8A02
F1-17	DB7	6085	4P30

6. Data Bufer

A. SA Settings for data buffer test.

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-7	
Stop	+ve	L3-7	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	-01 ROM Signature	-02ROM Signature
E3-18 (19)	D0	FC72	0P4H
E3-17 (18)	D1	FH21	1F5F
E3-16 (17)	D2	7A0H	37UU
E3-15 (16)	D3	UF65	U985
E3-14 (15)	D4	1PF4	758C
E3-13 (14)	D5	93FU	7U6C
E3-12 (13)	D6	6H72	8A02
E3-11 (12)	D7	6085	4P30

* The numbers in brackets are the pin assignments when an AM8304B is used as opposed to a 74LS245 *

7. Vector Generator Address Selector

A. SA Settings for VG Address Sel Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
K3-16	+5V	0003
K3-4		6U28
K3-12		4FCA
L3-9	VROM3	89CC
L3-10	VROM2	F501
L3-11	VROM1	P693
L3-12	VRAM	AA2A
F3-9	AM0	UUUU
F3-7	AM1	FFFF
F3-4	AM2	8484
F3-12	AM3	P763
H3-12	AM4	1U5P
H3-4	AM5	0356
H3-7	AM6	U759
H3-9	AM7	6F9A
J3-9	AM8	7791
J3-12	AM9	6321
J3-4	AM10	37C5

8. Vector Generator RAM

A. SA Settings for VG RAMTest

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
M5-3		98H1
M5-6		32U8
L5-4		37C6

9. Vector Generator ROM

A. SA Settings for VG ROM1 Test (R3)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-11	
Stop	+ve	L3-11	
Clock	-ve	C3-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
R3-24	+5V	826P
R3-9	DDMA0	2714
R3-10	DDMA1	9AA8
R3-11	DDMA2	5538
R3-13	DDMA3	C075
R3-14	DDMA4	546A
R3-15	DDMA5	74A3

R3-16	DDMA6	0475
R3-17	DDMA7	UP7F

C. SA Settings for ROM2 Test (N/P3)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-10	
Stop	+ve	L3-10	
Clock	-ve	C3-39	ϕ2

D Signatures

Logic Probe On IC	Signal Name	Signature
N/P3-9	DDMA0	CA58
N/P3-10	DDMA1	76A0
N/P3-11	DDMA2	5005
N/P3-13	DDMA3	0810
N/P3-14	DDMA4	CH7C
N/P3-15	DDMA5	98UF
N/P3-16	DDMA6	P859
N/P3-17	DDMA7	F9C2

10. Vector Generator Data Buffer

A. SA Settings for VG Data Buffer test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-10	
Stop	+ve	L3-10	
Clock	-ve	C2-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
R2-16 (17)	DB0	CA58
R2-17 (18)	DB1	76A0
R2-18 (19)	DB2	5005
R2-15 (16)	DB3	0810
R2-14 (15)	DB4	CH7C
R2-13 (14)	DB5	98UF
R2-12 (13)	DB6	P859
R2-11 (12)	DB7	F9C2

* The numbers in brackets are the pin assignments when an AM8304B is used as opposed to a 74LS245 *