ASTEROIDS

SIGNATURE ANALYSIS

GUIDE

Introduction

This guide is intended as an aid to troubleshooting the Asteroids video game PCB. The Signature Analyzer used to produce this guide was an HP5004a. If it is found that the signatures hold up for other makes/models of Signature Analyzers then please let me know and I can add some kind of compatibility list to the document.

To get the most out of the guide you'll need

Signature Analyzer (HP5004a)
Schematics for Asteroids
6502 NOP card (See the separate document 6502NOP for instructions on how to build your own NOP card)
IC Clips
Some jumper wires (3 or 4 should be sufficient)

The scope of the guide is limited in that it will not enable you to fault find the entire PCB. It should, however, be good for the following sections of the PCB:

Address Bus Buffers, Address Decoding Circuitry, Clock Circuit, Program ROMs and Data Buffer, Vector Generator Address Selector, Vector Generator RAM Select, Vector Generator ROMs and the Vector Generator Data Buffer.

The Clock Circuit test is very limited. The reason being is that I much prefer to check the clock chain with a scope. If you want to figure out the signatures for the Clock Circuit then pass on the information and I'll include it in the document. If you want a detailed description of these sections (and more) please refer to the Asteroids schematic / drawing package.

Using The Guide

For those of you who have used Atari Signature Analysis guides before then this should look familiar and there's probably no need to read through this section. For the rest of you, here's a quick run down. Every section should start with the settings for the Analyzer, something like this

A. SA Settings for xxxxx Test

Probe	Trigger	IC Pin	Test Pt.
Start	+ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	$\phi 2$

The probe column refers to either the Start, Stop or Clock probes from the Signature Analyzer.

The trigger column sets up the Start/Stop/Clock buttons on the front of the Analyzer. I have used –ve to indicate the negative going edge of the pulse (or the falling edge).
I have used +ve to indicate the positive going edge of the pulse (or the rising edge).
The IC Pin column refers to the point where the appropriate probe should be attached.
The Test Pt. column refers to an equivalent Test Point on the boards where the probe may be attached.

For example, in the example above the Start probe should be connected to pin 25 of IC C2. The Start button on the front of the Analyzer should be in the fully out position to indicate a positive going edge. Similarly, the Stop probe should be connected to the same IC/Pin as the Start probe but the Stop button on the Analyzer should be pressed in to indicate a negative going edge.

The section immediately following the set up procedure contains the signatures for that part of the test. The same structure for the Set Up was employed as explained below.

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
C1-20	+5V	0003
C1-9	AB0	UUUU
C1-12	AB1	FFFF

Here, with the Analyzer probe on pin 20 of IC C1 you should get a reading of 0003. On pin 9 of IC C1 you should get a reading of UUUU. And so on.

A signature denoted by an (*) indicates that signature may be unstable. Try taking the signature with a 1Kohm resistor connected between the probe tip and +5V.

Down To Business

One of the things I like about this testing method is that you don't need to have the PCB in the cabinet. If you prefer to work in the back of the cabinet then that's fine. If you have a bench/test area with a +5V PSU (as I'm sure most of you have), then you can sit comfortably at the bench. Simply connect Ground (pins 1 and 22 on the edge connector) and +5V (pins 2 and 21 on the edge connector) to the PCB, remove the game MPU and replace it with your NOP card and you're ready to start.

Just set up the Analyzer as indicated and start probing for those signatures. Always remember to have the Watchdog disabled as this will lead to permanently unstable signatures.

What To Do When You Find An Incorrect Signature

If you find a signature that doesn't match the guide, check your set up first. If your set up is OK then you'll need to trace the fault. Rather than having a long winded ramble from me it would be better to look at the following link on Al Kossow's page. If you haven't already had a look at his site then I'd definitely recommend having a look as it's a bit of a gold mine.

http://www.spies.com/arcade/TE/SigAnalNotes.pdf

After you've had a look through the document then you should know enough to start tracing the fault. It should also give you a bit more information on Signature Analysis in general.

Some Common Faults

The two most common faults I've come across are bad sockets and shorted traces. During the Signature Analysis the bad socket problem is highlighted by the fact that the signatures are unstable. You may get some stable and some not. When you get unstable signatures whilst doing the ROM tests it does not necessarily indicate a bad ROM. Reseating the ROM or replacing the socket is usually a good place to start. The problem of shorted traces is usually down to something being dragged across the board. Sometimes they can be quite hard to see but Signature Analysis shows it up quite good.

Disclaimer

If you toast yourself, your house, your dog, your family or more importantly your video game, then it's not my fault. You use the information contained in this guide at your own risk. Good luck.

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** Tie the Watchdog Disable test point to ground **

1. Address Lines

A. SA Settings for Address Buffer Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
C2-20	+5V	0003
C2-7	AB0	UUUU
C2-12	AB1	FFFF
C2-9	AB2	8484
C2-14	AB3	P763
C2-5	AB4	1U5P
C2-16	AB5	0356
C2-18	AB6	U759
C2-3	AB7	6F9A
B2-14	AB8	7791
B2-16	AB9	6321
B2-12	AB10	37C5
B2-7	AB11	6U28
B2-9	AB12	4FCA
C3-23	A13	4868
C3-24	A14	9UP1
C3-25	A15	0001

2. Address Decoding

A. SA Settings for Address Decoder Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
E4-4	SINP0	AF76
E4-5	SINP1	6913
E4-6	OPTS	13HP
E4-9	PMEM	3282
E4-10	VMEM	AH63
E4-11		7APA
E4-12	ZPAGE	P508
D6-10		3H01
C6-8		3H02
L3-5	PROM0	UH4P
L3-6	PROM1	A04H
L3-7	PROM2	86C1

C. SA Settings for Address Decoder Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C4-14	6MHz

** Tie R/W test point to ground **

D. Signatures

Logic Probe On IC	Signal Name	Signature
D6-14	+5V	00UP
D6-4		0066 **(*)**
E5-8		7U7C

L6-1	DMAGO	383U
L6-2	OUT	P759
L6-3	WDCLR	90P8
L6-4	EXPLODE	UA0P
L6-5	DMACNT	A43F
L6-6	THUMP	U5FA
L6-7	AUDIO	81F6
L6-9	NOISERESET	1A35

** Remove jumper from R/W test point **

3..Watchdog Circuit

A. SA Settings for Watchdog Circuit Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

** Tie L6-12 to ground **

B. Signatures

Logic Probe On IC	Signal Name	Signature
C6-14	+5V	0003
C6-6		752C
D5-6		0398
D5-8		0000

** Remove jumper from L6-12 **

4..Clock Circuit

A. SA Settings for Clock Circuit Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
B4-6		763H
B4-8	3KHz	8A4U
B4-10	12KHz	9720

5 ROM And Data Lines

A. SA Settings for ROM0 Test (F1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-5	
Stop	+ve	L3-5	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
F1-24	+5V	826P
F1-9	DB0	U83H
F1-10	DB1	C79H
F1-11	DB2	24U8
F1-13	DB3	6H6H
F1-14	DB4	41PA
F1-15	DB5	PP5A
F1-16	DB6	5857
F1-17	DB7	U454

C. SA Settings for ROM1 Test (D/E1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-6	
Stop	+ve	L3-6	
Clock	-ve	C3-39	ϕ2

D. Signatures

Logic Probe On IC	Signal Name	Signature
D/E1-9	DB0	8HCC
D/E1-10	DB1	673U
D/E1-11	DB2	AUU9
D/E1-13	DB3	0424
D/E1-14	DB4	F3AA
D/E1-15	DB5	6U88
D/E1-16	DB6	C7CF
D/E1-17	DB7	FFC3

E. SA Settings for ROM2 Test (C1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-7	
Stop	+ve	L3-7	
Clock	-ve	C3-39	ϕ2

F. Signatures

Logic Probe On IC	Signal Name	Signature
C1-9	DB0	15AP
C1-10	DB1	1F31
C1-11	DB2	F816
C1-13	DB3	0P0A
C1-14	DB4	F522
C1-15	DB5	9A7A
C1-16	DB6	7077
C1-17	DB7	3517

6. Data Buffer

A. SA Settings for data buffer test.

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-7	
Stop	+ve	L3-7	
Clock	-ve	C3-39	ϕ2

B. Signatures

Logic Probe On IC	Signal Name	Signature
E3-18 (19)	D0	15AP
E3-17 (18)	D1	1F31
E3-16 (17)	D2	F816
E3-15 (16)	D3	0P0A
E3-14 (15)	D4	F522
E3-13 (14)	D5	9A7A
E3-12 (13)	D6	7077
E3-11 (12)	D7	3517

** The numbers in brackets are the pin assignments when an AM8304B is used as opposed to a 74LS245 **

7. Vector Generator Address Selector

A. SA Settings for VG Address Sel Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C2-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature

K3-16	+5V	0003
K3-4	AM11	6U28
K3-12	AM12	4FCA
L3-10	VROM2	F501
L3-12	VRAM	AA2A
F3-9	AM0	UUUU
F3-7	AM1	FFFF
F3-4	AM2	8484
F3-12	AM3	P763
H3-12	AM4	1U5P
H3-4	AM5	0356
H3-7	AM6	U759
H3-9	AM7	6F9A
J3-9	AM8	7791
J3-12	AM9	6321
J3-4	AM10	37C5

8. Vector Generator RAM

A. SA Settings for VG Ram Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C3-25	
Stop	-ve	C3-25	
Clock	-ve	C3-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
M5-3		98H1
M5-6		32U8
L5-4		37C6

9. Vector Generator ROM

A. SA Settings for VG ROM Test (R2)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-10	
Stop	+ve	L3-10	
Clock	-ve	C3-39	ϕ2

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
N/P3-24	+5V	826P
N/P3-9	DDMA0	1F07
N/P3-10	DDMA1	5AU1
N/P3-11	DDMA2	U2A9
N/P3-13	DDMA3	5HH6
N/P3-14	DDMA4	HUF5
N/P3-15	DDMA5	5690
N/P3-16	DDMA6	9H79
N/P3-17	DDMA7	5716

10. Vector Generator Data Buffer

A. SA Settings for VG Data Buffer test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L3-10	
Stop	+ve	L3-10	
Clock	-ve	C3-39	$\phi 2$

** Tie K3-1 to ground **

B Signatures

Logic Probe On IC	Signal Name	Signature
R2-16 (17)	DB0	1F07
R2-17 (18)	DB1	5AU1
R2-18 (19)	DB2	U2A9
R2-15 (16)	DB3	5HH6
R2-14 (15)	DB4	HUF5
R2-13 (14)	DB5	5690
R2-12 (13)	DB6	9H79
R2-11 (12)	DB7	5716

* The numbers in brackets are the pin assignments when an AM8304B is used as opposed to a 74LS245. The AM8304B is located at P2 but the pin numbers in brackets still stand *