

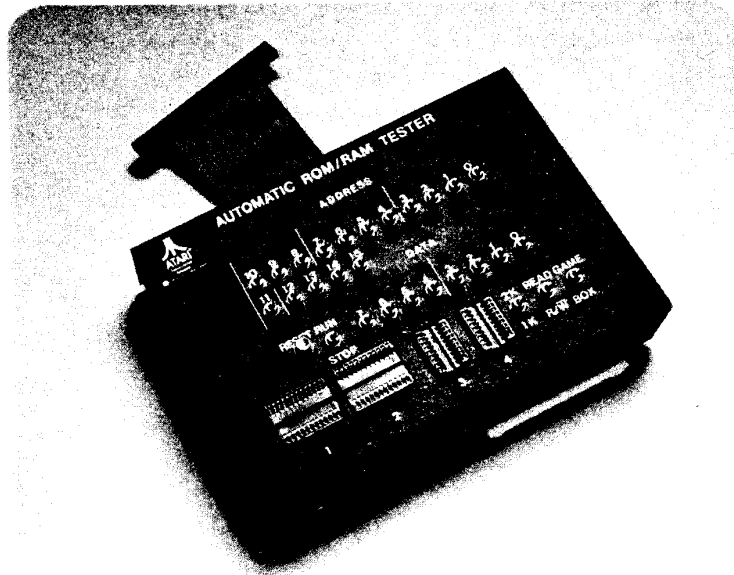
TM-120  
1st printing

INSTRUCTION MANUAL

AUTOMATIC ROM/RAM TESTER

Including Memory Maps for  
Atari Microprocessor Games

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## INTRODUCTION

### 1. Uses of ROM/RAM Tester

The Atari Automatic ROM/RAM Tester may be used in three different methods of operation.

- A. The tester may be used as a manual switch box. This allows the operator to select a particular address location, via the address switches (A0-A15) on the tester control panel. The operator can then write data to this specific address, via data switches (D0-D7), or read data from this address, via data LEDs (D0-D7).
- B. The tester may be used to generate address locations automatically. This method is most useful for checking large blocks of RAM, such as Display Memory or Base Page Memory. In this mode, the operator presets the address switches to a particular address. When initiated, the tester will automatically begin sequencing up through all addresses from that point, until the operator manually stops the sequence. The tester may be used to either read or write in this mode. In the read mode, it can also be used to automatically verify incoming data against the setting of the Data switches (D0-D7) on the tester control panel.
- C. The tester may also be used to compare a suspect PCB ROM with a known good test ROM, which can be installed in a socket in the control panel of the tester. The tester will automatically scan the entire address range of the game PCB ROM, and compare its data with that of the Test ROM. The test will automatically stop if the data in any address location does not compare with the ROM in the tester.

### 2. MEMORY MAP

Memory maps are provided at the back of this manual for most microprocessor games made by Atari. The memory map is a table that defines the inputs and outputs of the microprocessor. The memory map lists the hexadecimal-codes addresses (see Hexadecimal Code Section) used for the programming of that particular game.

### 3. HEXADECIMAL CODE

In our everyday life we use base 10 or the decimal system for counting. We learn this system easily because we have ten fingers. A computer can't count to ten like we can, since it doesn't have ten fingers.

In any digital computer, there are two logic states, high (or 1) and low (or 0). Therefore, the digital computer can count only in binary or base 2. The binary system is easy to learn by

people, but it is an extremely cumbersome system for communication between two persons. For example, the number 2,641 in base 10 would be written 101001010001 in base 2 or binary. Yes, it is cumbersome. What we need is a number system that is convenient for both the computer and people.

Because of this need, the hexadecimal system or base 16 was developed. The number 101001010001 in base 2 is written A51 in hexadecimal. As can easily be seen, hexadecimal includes both alpha and numeric characters for digit designators. One hexadecimal digit is equivalent to four binary digits.

The tester has sixteen ADDRESS switches. Notice that these switches are divided into four groups of four switches each. Each group of four switches has sixteen possible ways of being set. This is demonstrated by representing the actual switch settings with ones and zeroes in the center column (see Table 1-1). A one means that the switch is ON and a zero means the switch is OFF. Of course, this column also represents the binary number for that switch setting. The left column is the decimal equivalent and the right column is the hexadecimal equivalent for the binary number.

Table 1-1  
Conversion from Decimal Numbering System to Binary and Hexadecimal

DECIMAL	BINARY	HEXADECIMAL
	SWITCH 3 2 1 0	
0	0 0 0 0	0
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 0 0 0	8
9	1 0 0 1	9
10	1 0 1 0	A
11	1 0 1 1	B
12	1 1 0 0	C
13	1 1 0 1	D
14	1 1 1 0	E
15	1 1 1 1	F

Understanding this, you are now ready to convert a hexadecimal number into a binary number. As an example, take the hexadecimal numbers 3800 and 4C9F and convert them into binary as follows:

Hex		
3800	=	0011 1000 0000 0000
Hex		
4C9F	=	0100 1100 1001 1111

## B. MODES OF OPERATION OF ROM/RAM TESTER

### 1. Manual Mode

In the manual mode of operation, the game PCB's address and data lines are all statically controlled via the address (A0-A15) and data (D0-D7) switches on the tester control panel. This mode is useful for locating shorts between traces, bad buffers between the MPU and the "outside world", faulty address decoding circuits, etc. The operator, in this mode, can basically simulate step by step any transfer of data on the MPU data bus (D0-D7), either by writing data to the peripheral circuitry (using data switches D0-D7) or reading data from the peripheral circuitry (using data LEDs D0-D7).

To function in the manual mode, the RUN/STOP switch should be set to STOP. The READ/R $\bar{W}$  switch should be set to READ if the operator is trying to read data from the game PCB via the data LEDs. It should be set to R $\bar{W}$  if the operator is trying to write data to the game PCB via the data switches. The GAME/BOX switch should be set to GAME if the operator wants the data LEDs to reflect data being read from the game PCB. It should be set to BOX if the operator wants the data LEDs to reflect the actual data switches as set on the tester. The RESET button and the 1K/2K switch are not used in the manual mode of operation.

CAUTION: It is important that there are no ROMs in any of the test sockets on the tester control panel during this manual mode of operation. Failure to remove any ROMs from these sockets before entering the manual mode could result in damage to the ROM.

### 2. Automatic Mode

The automatic mode of operation provides the capability of quickly checking large blocks of ROM and RAM via an automatic addressing sequence generated by the ROM/RAM tester. To use this mode to check RAM, the operator first writes a known data bit pattern into all RAM locations, using data switches D0-D7 to set this bit pattern. The same RAM locations can then be read by the ROM/RAM tester, and the RAM data outputs are compared with the tester's data switch settings. If what was written into the RAM is ever in conflict with what is read back from the RAM, the tester will automatically stop, and display the address and data bit which is in error. For details on performing this test, see RAM TEST.

To use the ROM/RAM tester to verify a game PCB ROM, the operator is required to have a known good test ROM. (This test ROM should have an identical Atari part number as the ROM under test). In this mode, the tester automatically compares the game PCB ROM's data output with that of the test ROM. Once initiated, this test will sequence over and over again until the operator stops the test, or until an error is found. If an error is recognized, the tester will stop and display the address and data bit in error. For details on performing this test, see ROM TEST.

## C. USING THE ROM/RAM TESTER

### 1. Game PCB Preparation

- a. Remove MPU (microprocessor) from the game PCB.
- b. Prepare game PCB as instructed in PCB PREPARATION box at top of game PCB Memory Map.
- c. Plug tester 50-pin connector onto game PCB, making sure 50-pin connector side marked TOP is on top side of game PCB.

### 2. Address & Data Bus Tests

- a. Apply power to game PCB, then check all regulated voltages on the game PCB.
- b. Set READ/R/W switch to R/W and RUN/STOP switch to STOP. Stagger all ADDRESS and DATA switches on, off, on, off, etc. With logic probe or oscilloscope, check each buffered address and data line on the game PCB to ensure that logic is same as switches set on tester.

### 3. RAM Test

- a. Set READ/R/W switch to R/W, RUN/STOP switch to STOP, and stagger DATA switches on, off, on, off, etc.
- b. Refer to game PCB memory map and set ADDRESS switches to lowest RAM address.
- c. Set RUN/STOP switch to RUN. Let ADDRESS LEDs count up to RAM's highest address, then set RUN/STOP switch to STOP.
- d. Set READ/R/W switch to READ, then set RUN/STOP switch to RUN. ADDRESS LEDs should cycle from lowest to highest RAM address until you set RUN/STOP switch to STOP. If ADDRESS LEDs stop counting before the last RAM address, there is a RAM failure at the address at which the tester stopped counting.
- e. Set RUN/STOP switch to STOP, READ/R/W switch to R/W, then stagger DATA switches off, on, off, on, etc.
- f. Set RUN/STOP switch to RUN. Let ADDRESS LEDs count up to RAM's highest address, then set RUN/STOP switch to STOP.
- g. Set READ R/W switch to READ, then set RUN/STOP switch to RUN. ADDRESS LEDs should cycle from lowest to highest RAM address, until RUN/STOP switch is set to STOP, If ADDRESS LEDs stop counting before last RAM address, there is a RAM failure at the address at which the tester stopped counting.

#### 4. ROM TEST

- a. Refer to game PCB memory map to determine which ROM socket on tester to use for inserting your known-to-be-good test ROM. In general, if the ROM under test is of the EA 4600 type (+5V is on pin 9 and ground is on PIN 1, i.e. SPRINT II), the tester ROM socket #1 should be used. If the ROM under test is of the 8316 E type (+5V is on pin 24 and ground is on pin 12, i.e. MIDDLE EARTH), the tester ROM socket #2 should be used. If the memory under test is composed of PROM (18-pin chips, i.e. TIME 2000), the tester ROM sockets #3 and 4 should be used. Socket 3 is the LSB test socket (D0-D3) and socket 4 is the MSB test socket (D4 thru D7).

CAUTION: When inserting a known-to-be-good test ROM into one of the tester sockets, it is critical that you ensure you are inserting the proper ROM into the proper socket and that pin 1 on the ROM is lined up with Pin 1 on the socket. Failure to observe this caution will probably result in a known-to-be-bad test ROM.

- b. Set 1K/2K switch to 2K if known to be good Test ROM is in socket 1 or 2. If using socket 3 and 4, you must first determine if the PROM chips under test are of a size of 1K x 4 (in which case you set switch to 1K) or of 2K x 4 (in which case you set switch to 2K).

This information should be contained in the Memory Map section of the appropriate game.

NOTE: One way of determining the size of the PROM under test is by the number of address inputs shown on the game schematic. A 1K Prom will have 10 address inputs (A0 thru A9) and two CE inputs (on pins 8 and 10). A 2K Prom will have 11 address inputs (A0 thru A10) and one CE input (on pin 10).

- c. Set READ/R/ $\bar{W}$  switch to the center position, the RUN/STOP switch to STOP; then set ADDRESS switches to lowest address for the known to be good test ROM. Check with a logic probe to make sure the ROM under test is enabled on the game PCB.
- d. NOW insert test ROM into appropriate socket.
- e. Set RUN/STOP switch to RUN, then press RESET button. ADDRESS LEDs should cycle from lowest to highest ROM address, again, and again, until RUN/STOP switch is set to STOP. If ADDRESS LEDs stop counting, there is a ROM failure at the address at which the tester stopped counting.

5. Video Display Test (Not applicable to Pinball)

- a. Prepare PCB as indicated in PCB PREPARATION box above VIDEO DISPLAY line on memory map.
- b. Set ADDRESS switches to VIDEO ADDRESS as indicated on game PCB memory map.
- c. Set READ/R $\bar{W}$  switch to R $\bar{W}$ .
- d. Set RUN/STOP switch to RUN.
- e. Set DATA switches as indicated on game PCB memory map. Alpha, numerics, and playfield characters displayed on TV monitor can be changed by writing different combinations of data to the appropriate addresses.
- f. When convinced alpha, numerics, and playfield characters are displayed properly, refer to PCB PREPARATION for VIDEO DISPLAY test box on game PCB memory map and follow those procedures in reverse.

Switch Line Test

Switch lines are actually the inputs to the microprocessor from the front panel controls on the game. These may be tested individually by selecting the memory map address information and setting the address switches on the RAM/ROM tester to the corresponding settings. The memory map also contains information which indicates what data line LED on the RAM/ROM tester will be used to indicate an actuated switch on data line.

The advantage in this case is that any latches, multiplexers or other supporting logic will be set up to look at only the input switch under test. All the address lines can be controlled to check each device in the circuit and to follow the flow of information from the switch to the data line.

This test is done using the manual mode of operation.

Latch Tests

Latches are used to temporarily store data information so it can be put to some practical use. To turn on a flipper coil in a pinball game, latches are used. In order to do this, take the address information in the memory map and set the address switches accordingly. The data information needed to turn the device on and off is also on the map. This test is done using the manual mode of operation.



D. GAME MEMORY MAPS

THE ATARIANS™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Cut and lift D4 pin 2 and B10 pin 4.

RAM ADDRESS

0000 to 01FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 0 (E1)	006990	7000 to 73FF	3
PROM 1 (E7)	006991	7000 to 73FF	4
PROM 2 (E2)	006992	7400 to 77FF	3
PROM 3 (E8)	006993	7400 to 77FF	4
PROM 4 (E4)	006994	7800 to 7BFF	3
PROM 5 (E5)	006995	7800 to 7BFF	4
PROM 6 (E3)	006996	7C00 to 7FFF	3
PROM 7 (E6)	006997	7C00 to 7FFF	4

Set READ/R/W to center position, STOP/RUN to RUN, 1K/2K to 1K.

Test PROMs two at a time as indicated by brackets.

SWITCH TEST	HEX ADDRESS	DATA LED
Toggle #1 Prog SW1	(A) 200B	D7
Toggle #2 Prog SW1	(A) 200A	D7
Toggle #3 Prog SW1	(A) 2009	D7
Toggle #4 Prog SW1	(A) 2008	D7
Toggle #5 Prog SW1	(A) 200F	D7
Toggle #6 Prog SW1	(A) 200E	D7
Toggle #7 Prog SW1	(A) 200D	D7
Toggle #8 Prog SW1	(A) 200C	D7
Toggle #1 Prog SW2	(A) 2003	D7
Toggle #2 Prog SW2	(A) 2002	D7
Toggle #3 Prog SW2	(A) 2001	D7
Toggle #4 Prog SW2	(A) 2000	D7
Toggle #5 Prog SW2	(A) 2007	D7
Toggle #6 Prog SW2	(A) 2006	D7
Toggle #7 Prog SW2	(A) 2005	D7
Toggle #8 Prog SW2	(A) 2004	D7
Playfield SW #4	(A) 201B	D7
Playfield SW #3	(A) 201A	D7
Playfield SW #2	(A) 2019	D7
Playfield SW #1	(A) 2018	D7
Playfield SW #8	(A) 201F	D7
Playfield SW #7	(A) 201E	D7
Playfield SW #6	(A) 201D	D7
Playfield SW #5	(A) 201C	D7

SWITCH TEST	HEX ADDRESS	DATA LED
Tilt (Slam)	(A) 2013	D7
Start	(A) 2012	D7
Coin 2	(A) 2011	D7
Coin 1	(A) 2010	D7
Tilt (Cabinet)	(A) 2016	D7
Tilt (Pendulum)	(A) 2015	D7
Tilt	(A) 2014	D7
A (on <u>ATARI</u> Sol)	(A) 202B	D7
Slingshot, right	(A) 202A	D7
Slingshot, left	(A) 2029	D7
Pop bumper, center	(A) 2028	D7
I (on <u>ATARI</u> Sol)	(A) 202F	D7
R (on <u>ATARI</u> Sol)	(A) 202E	D7
A (on <u>ATARI</u> Sol)	(A) 202D	D7
T (on <u>ATARI</u> Sol)	(A) 202C	D7
Open left gate	(A) 2023	D7
10 Points	(A) 2022	D7
Advance Bonus	(A) 2021	D7
Playfield SW #9	(A) 2021	D7
Pop bumper, right	(A) 2027	D7
Pop bumper, left	(A) 2026	D7
Close Gates	(A) 2025	D7
Open right gate	(A) 2024	D7
Flipper left	(A) 2033	D7
Outhole kicker	(A) 2032	D7
Hole kicker, right	(A) 2031	D7
Hole kicker, left	(A) 2030	D7
Flipper, right	(A) 2034	D7
Replace Bit 0	(A) 2046	D7
Replace Bit 1	(A) 204D	D7
Replace Bit 2	(A) 204E	D7
Replace Bit 3	(A) 204F	D7

PREPARATION FOR LATCH TEST

Solder B10 pin 4 back down on PCB.

LATCH TEST (Solenoids)	HEX ADDRESS	DATA SWITCH
Right flipper	(A)108C	D0
Left flipper	(A)108C	D1
Right gate	(A)108C	D2
Left gate	(A)1083	D3
Atari	(A)1088	D4
Right slingshot	(A)108C	D4
Right hole kicker	(A)1088	D5
Left slingshot	(A)108C	D5
Left hole kicker	(A)1088	D6
Outhole	(A)108C	D6
Total plays	(A)1088	D7
Time counter	(A)108C	D7
Right pop bumper	(A)1084	D4
Left pop bumper	(A)1084	D5
Special counter	(A)1080	D6
Center pop bumper	(A)1084	D6
Lamps	(A)1000	D0
Lamps	(A)1000	D1
Lamps	(A)1000	D2
Lamps	(A)1000	D3
Lamps	(A)1000	D4
Lamps	(A)1000	D5
Lamps	(A)1000	D6
Lamps	(A)1000	D7
Lamps	(A)1004	D0
Lamps	(A)1004	D1
Lamps	(A)1004	D2
Lamps	(A)1004	D3
Lamps	(A)1004	D4
Lamps	(A)1004	D5
Lamps	(A)1004	D6
Lamps	(A)1004	D7
Lamps	(A)1008	D0
Lamps	(A)1008	D1
Lamps	(A)1008	D2
Lamps	(A)1008	D3
Lamps	(A)1008	D4
Lamps	(A)1008	D5
Lamps	(A)1008	D6
Lamps	(A)1008	D7

LATCH TEST (Solenoids), cont.	HEX ADDRESS	DATA SWITCH
Lamps	(A) 100C	D0
Lamps	(A) 100C	D1
Lamps	(A) 100C	D2
Lamps	(A) 100C	D3
Lamps	(A) 100C	D4
Lamps	(A) 100C	D5
Lamps	(A) 100C	D6
Lamps	(A) 100C	D7

AUDIO TEST	HEX ADDRESS	DATA SWITCH
Audio Reset	(A) 6000	D0
Audio Enable	(A) 3000	D0
Latch Bit 0	(A) 1088	D0
Latch Bit 1	(A) 1088	D1
Latch Bit 2	(A) 1088	D2
Latch Bit 3	(A) 1088	D3
Latch Bit 0	(A) 1080	D0
Latch Bit 1	(A) 1080	D1
Latch Bit 2	(A) 1080	D2
Latch Bit 3	(A) 1080	D3

TO END TESTING

Solder down D4 pin 2 back on PCB.  
 Replace MPU in socket.

TIME 2000™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Cut and lift D4 pin 2 and B10 pin 4 on PCB.

RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET	
PROM 0 (E1)	020046	7000 to 73FF	3	Set READ/R/W to center position, STOP/RUN to RUN, and 1K/2K to 1K.
PROM 1 (E7)	020047	7000 to 73FF	4	
PROM 2 (E2)	020048	7400 to 77FF	3	
PROM 3 (E8)	020049	7400 to 77FF	4	
PROM 4 (E4)	020050	7800 to 7BFF	3	Test PROMs two at a time as indicated by brackets.
PROM 5 (E5)	020051	7800 to 7BFF	4	
PROM 6 (E3)	020052	7C00 to 7FFF	3	
PROM 7 (E6)	020053	7C00 to 7FFF	4	

SWITCH TEST

HEX ADDRESS

Toggle #1 Prog SW1	(A) 200B
Toggle #2 Prog SW1	(A) 200A
Toggle #3 Prog SW1	(A) 2009
Toggle #4 Prog SW1	(A) 2008
Toggle #5 Prog SW1	(A) 200F
Toggle #6 Prog SW1	(A) 200E
Toggle #7 Prog SW1	(A) 200D
Toggle #8 Prog SW1	(A) 200C
Toggle #1 Prog SW2	(A) 2003
Toggle #2 Prog SW2	(A) 2002
Toggle #3 Prog SW2	(A) 2001
Toggle #4 Prog SW2	(A) 2000
Toggle #5 Prog SW2	(A) 2007
Toggle #6 Prog SW2	(A) 2006
Toggle #7 Prog SW2	(A) 2005
Toggle #8 Prog SW2	(A) 2004
Tilt (Slam) (ST4)	(A) 2013
Start (ST3)	(A) 2012
Coin 2 (ST2)	(A) 2011
Coin 1 (ST1)	(A) 2010
Right Flipper	(A) 2023
Left Flipper	(A) 2022
Tilt, pendulum	(A) 2021
Tilt, cabinet	(A) 2020

Operation of all switches will be indicated on data LED 7

SWITCH TEST, cont.	HEX ADDRESS
Right hole kicker	(A) 2027
Center hole kicker	(A) 2026
Right pop bumper	(A) 2025
Left pop bumper	(A) 2024
2000 + Advance lit clock	(A) 203B
Center target	(A) 203A
100 + Advance PM	(A) 2039
Lower Drop target	(A) 2038
50 + change	(A) 203E
Triple Advance PM	(A) 203D
Triple Advance PM	(A) 203C
10 Pts. + ON AM	(A) 2033
10 Pts. + Change	(A) 2032
Right slingshot	(A) 2031
Left slingshot	(A) 2030
Upper drop target	(A) 2037
100 Pts. + Advance AM	(A) 2036
Outhole kicker	(A) 2035
10 Pts. + ON PM	(A) 2034
Right side drain	(A) 204B
Left side drain	(A) 204A
Hex code & switch	(A) 204F
Hex code & switch	(A) 204E
Hex code & switch	(A) 204D
Hex code & switch	(A) 204C

TO END SWITCH TEST

Solder B10 pin 4 back down.

PREPARATION FOR LATCH TEST

Solder B10 pin 4 back down.

LATCH TEST (Solenoids)	HEX ADDRESS	DATA SWITCH
Right hole kicker	(A) 1088	D4
Right slingshot	(A) 108C	D4
Center hole kicker	(A) 1088	D5
Left slingshot	(A) 108C	D5
Gate	(A) 1088	D6
Outhole kicker	(A) 108C	D6
Right center flipper	(A) 1088	D7
Left flipper	(A) 108C	D7
Right pop bumper	(A) 1084	D4
Left pop bumper	(A) 1084	D5
Left center flipper	(A) 1080	D6
Lower drop target	(A) 1084	D6
Right flipper	(A) 1080	D7
Upper drop target	(A) 1084	D7
Lamps	(A) 1000	D0
Lamps	(A) 1000	D1
Lamps	(A) 1000	D2
Lamps	(A) 1000	D3
Lamps	(A) 1000	D4
Lamps	(A) 1000	D5
Lamps	(A) 1000	D6
Lamps	(A) 1000	D7
Lamps	(A) 1004	D0
Lamps	(A) 1004	D1
Lamps	(A) 1004	D2
Lamps	(A) 1004	D3
Lamps	(A) 1004	D4
Lamps	(A) 1004	D5
Lamps	(A) 1004	D6
Lamps	(A) 1004	D7
Lamps	(A) 1008	D0
Lamps	(A) 1008	D1
Lamps	(A) 1008	D2
Lamps	(A) 1008	D3
Lamps	(A) 1008	D4
Lamps	(A) 1008	D5
Lamps	(A) 1008	D6
Lamps	(A) 1008	D7
Lamps	(A) 100C	D0
Lamps	(A) 100C	D1
Lamps	(A) 100C	D2
Lamps	(A) 100C	D3
Lamps	(A) 100C	D4
Lamps	(A) 100C	D5
Lamps	(A) 100C	D6
Lamps	(A) 100C	D7



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AUDIO TEST	HEX ADDRESS	DATA SWITCH
Audio Reset	(A) 6000	
Audio Enable	(A) 3000	
Latch Bit 0	(A) 1088	D0
Latch Bit 1	(A) 1088	D1
Latch Bit 2	(A) 1088	D2
Latch Bit 3	(A) 1088	D3
Latch Bit 0	(A) 1080	D0
Latch Bit 1	(A) 1080	D1
Latch Bit 2	(A) 1080	D2
Latch Bit 3	(A) 1080	D3

TO END TESTING

Solder D4 pin 2 down on PCB.  
Replace MPU in socket.

AIRBORNE AVENGER™ MEMORY MAP

PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Cut and lift D4 pin 2 and B10 pin 4.

RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 0 (E1)	020244	7000 to 73FF	3
PROM 1 (E7)	020250	7000 to 73FF	4
PROM 2 (E2)	020245	7400 to 77FF	3
PROM 3 (E8)	020251	7400 to 77FF	4
PROM 4 (E4)	020247	7800 to 7BFF	3
PROM 5 (E5)	020248	7800 to 7BFF	4
PROM 6 (E3)	020246	7C00 to 7FFF	3
PROM 7 (E6)	020249	7C00 to 7FFF	4
ROM (E00)	020288	7000 to 77FF	1
ROM 0 (E0)	020287	7800 to 7FFF	1

SET READ/R/W to center position, STOP/RUN to RUN and 1K/2K to 1K.

Test PROMs two at a time as indicated by brackets.

SWITCH TEST	HEX ADDRESS	DATA LED
Toggle #1 Prog SW1	(A) 200B	D7
Toggle #2 Prog SW1	(A) 200A	D7
Toggle #3 Prog SW1	(A) 2009	D7
Toggle #4 Prog SW1	(A) 2008	D7
Toggle #5 Prog SW1	(A) 200F	D7
Toggle #6 Prog SW1	(A) 200E	D7
Toggle #7 Prog SW1	(A) 200D	D7
Toggle #8 Prog SW1	(A) 200C	D7
Toggle #1 Prog SW2	(A) 2003	D7
Toggle #2 Prog SW2	(A) 2002	D7
Toggle #3 Prog SW2	(A) 2001	D7
Toggle #4 Prog SW2	(A) 2000	D7
Toggle #5 Prog SW2	(A) 2007	D7
Toggle #6 Prog SW2	(A) 2006	D7
Toggle #7 Prog SW2	(A) 2005	D7
Toggle #8 Prog SW2	(A) 2004	D7
Slam (ST4)	(A) 2013	D7
Start (ST3)	(A) 2012	D7
Coin 2 (ST2)	(A) 2011	D7
Coin 1 (ST1)	(A) 2010	D7
Right flipper	(A) 2023	D7
Left flipper	(A) 2022	D7
Tilt, pendulum	(A) 2021	D7
Tilt, cabinet	(A) 2020	D7

SWITCH TEST , cont.	HEX ADDRESS	DATA LED
Target 1	(A) 2027	D7
Target 2	(A) 2026	D7
Target 3	(A) 2025	D7
Target 4	(A) 2024	D7
Upper left thumper	(A) 203B	D7
Upper right thumper	(A) 203A	D7
Lower right thumper	(A) 2039	D7
Left ball eject hole	(A) 2038	D7
Right ball eject hole	(A) 203F	D7
Left eject pocket	(A) 203E	D7
Right eject pocket	(A) 203D	D7
Spinning target	(A) 203C	D7
Rollover No. 1	(A) 2033	D7
Rollover No. 2	(A) 2032	D7
Rollover No. 3	(A) 2031	D7
Rollover No. 5	(A) 2037	D7
Rollover No. 6	(A) 2036	D7
Rollover No. 7	(A) 2035	D7
Rollover No. 8	(A) 2034	D7
Rollthru upper right	(A) 204B	D7
Rollover "B" center	(A) 204A	D7
Captive ball rollovers	(A) 2049	D7
50 Points & letter adv.	(A) 2048	D7
Hex coded switch 0	(A) 204F	D7
Hex coded switch 1	(A) 204E	D7
Hex coded switch 2	(A) 204D	D7
Hex coded switch 3	(A) 204C	D7
Outhole kicker	(A) 2043	D7
50 Points	(A) 2042	D7
10 Points	(A) 2041	D7
Left slingshot	(A) 2048	D7
Right slingshot	(A) 2047	D7

PREPARATION FOR LATCH TEST

Solder B10 pin 4 down. Lift A1 pin 1.

LATCH TEST (Solenoids)	HEX ADDRESS	DATA SWITCH
Right ball eject	(A)1088	D4
Right slingshot	(A)108C	D4
Left ball eject	(A)1088	D5
Left slingshot	(A)108C	D5
Gate	(A)1088	D6
Outhole kicker	(A)108C	D6
Right eject pocket	(A)1088	D7
Left flipper	(A)108C	D7
Upper right thumper	(A)1084	D4
Upper left thumper	(A)1084	D5
Left eject pocket	(A)1080	D6
Extra ball meter	(A)1084	D6
Right flipper	(A)1080	D7
Lower right thumper	(A)1084	D7
Lamps	(A)1000	D0
Lamps	(A)1000	D1
Lamps	(A)1000	D2
Lamps	(A)1000	D3
Lamps	(A)1000	D4
Lamps	(A)1000	D5
Lamps	(A)1000	D6
Lamps	(A)1000	D7
Lamps	(A)1004	D0
Lamps	(A)1004	D1
Lamps	(A)1004	D2
Lamps	(A)1004	D3
Lamps	(A)1004	D4
Lamps	(A)1004	D5
Lamps	(A)1004	D6
Lamps	(A)1004	D7
Lamps	(A)1008	D0
Lamps	(A)1008	D1
Lamps	(A)1008	D2
Lamps	(A)1008	D3
Lamps	(A)1008	D4
Lamps	(A)1008	D5
Lamps	(A)1008	D6
Lamps	(A)1008	D7
Lamps	(A)100C	D0
Lamps	(A)100C	D1
Lamps	(A)100C	D2
Lamps	(A)100C	D3
Lamps	(A)100C	D4
Lamps	(A)100C	D5
Lamps	(A)100C	D6
Lamps	(A)100C	D7

Chips not stuffed.

Chips not stuffed.

AUDIO TEST	HEX ADDRESS	DATA SWITCH
Audio Reset	(A) 6000	
Audio Enable	(A) 3000	
Latch Bit 0	(A) 1088	D0
Latch Bit 1	(A) 1088	D1
Latch Bit 2	(A) 1088	D2
Latch Bit 3	(A) 1088	D3
Latch Bit 0	(A) 1080	D0
Latch Bit 1	(A) 1080	D1
Latch Bit 2	(A) 1080	D2
Latch Bit 3	(A) 1080	D3

TO END TESTING

Solder D4 pin 2 and A1 pin 1 back down on PCB.  
 Replace MPU in socket.

MIDDLE EARTH™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Cut and lift D4 pin 2 and B10 pin 4.

RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

ROM ADDRESS

Domestic Version ROM Set

ROM#	PART #	ADDRESS	SOCKET
ROM 0 (E0)	020608-01	7800 to 7FFF	1
ROM 00 (E00)	020609-01	7000 to 77FF	1

Set READ/R/W to center position, STOP/RUN to RUN, 1K/2K to 2K

Updated Domestic Version ROM Set

ROM#	PART #	ADDRESS	SOCKET
ROM 0 (E0)	020608-01	7800 to 7FFF	1
ROM 00 (E00)	020609-02	7000 to 77FF	1

German Version ROM Set

ROM#	PART #	ADDRESS	SOCKET
ROM 0 (E0)	020856-01	7800 to 7FFF	1
ROM 00 (E00)	020855-02	7000 to 77FF	1

SWITCH TEST

HEX ADDRESS

DATA LED

Toggle #1 Prog SW1	(A) 200B	D7
Toggle #2 Prog SW1	(A) 200A	D7
Toggle #3 Prog SW1	(A) 2009	D7
Toggle #4 Prog SW1	(A) 2008	D7
Toggle #5 Prog SW1	(A) 200F	D7
Toggle #6 Prog SW1	(A) 200E	D7
Toggle #7 Prog SW1	(A) 200D	D7
Toggle #8 Prog SW1	(A) 200C	D7
Toggle #1 Prog SW2	(A) 2003	D7
Toggle #2 Prog SW2	(A) 2002	D7
Toggle #3 Prog SW2	(A) 2001	D7
Toggle #4 Prog SW2	(A) 2000	D7
Toggle #5 Prog SW2	(A) 2007	D7
Toggle #6 Prog SW2	(A) 2006	D7
Toggle #7 Prog SW2	(A) 2005	D7
Toggle #8 Prog SW2	(A) 2004	D7
Slam	(A) 2013	D7
Start	(A) 2012	D7
Coin 2	(A) 2011	D7
Coin 1	(A) 2010	D7
Right flipper	(A) 2023	D7
Left flipper	(A) 2022	D7
Tilt (pendulum)	(A) 2021	D7
Tilt (cabinet)	(A) 2020	D7

SWITCH TEST, cont.	HEX ADDRESS	DATA LED
Right pop bumper	(A) 2027	D7
Left pop bumper	(A) 2026	D7
Right upper rollover	(A) 2025	D7
Left upper rollover	(A) 2024	D7
Left drain	(A) 203B	D7
Left slingshot	(A) 203A	D7
Right slingshot	(A) 2039	D7
Outhole kicker	(A) 2038	D7
Rollthru rollover	(A) 203F	D7
Target in front of rollthru	(A) 203E	D7
Target NW of left pop	(A) 203D	D7
Target SW of left pop	(A) 203C	D7
Right drain	(A) 2033	D7
Lower inner ball lane rollover	(A) 2032	D7
Right lower playfield	(A) 2031	D7
Left lower rollover	(A) 2030	D7
Upper drop target #2	(A) 2037	D7
Upper drop target #1	(A) 2036	D7
Target NE of right pop	(A) 2035	D7
Target NW of right pop	(A) 2034	D7
Lower drop target #4	(A) 204B	D7
Lower drop target #3	(A) 204A	D7
Lower drop #2	(A) 2049	D7
Lower drop #1	(A) 2048	D7
Replay bit 3	(A) 204F	D7
Replay bit 2	(A) 204E	D7
Replay bit 1	(A) 204D	D7
Replay bit 0	(A) 204C	D7
Upper drop #3	(A) 2043	D7
Right spinning target	(A) 2042	D7
Upper drop #4	(A) 2041	D7
All 10 Pts.	(A) 2040	D7
Upper drop #5	(A) 2047	D7
Left spinner	(A) 2046	D7
Switch in back of drop	(A) 2045	D7
Lower drop #5	(A) 2044	D7

PREPARATION FOR LATCH TEST

Solder B10 pin 4 back down on PCB.  
Also lift A1 pin 1.

LATCH TEST (Solenoids)	HEX ADDRESS	DATA SWITCHES
Left upper flipper	(A)1088	D4
Left slingshot	(A)108C	D4
Right upper flipper	(A)1088	D5
Right slingshot	(A)108C	D5
Right lower flipper	(A)1088	D6
Upper drop target	(A)108C	D6
Left lower flipper	(A)1088	D7
Lower drop target	(A)108C	D7
Left thumper	(A)1084	D5
Extra ball meter	(A)1084	D6
Right thumper	(A)1080	D7
Outhole kicker	(A)1084	D7
Lamps	(A)1000	D0
Lamps	(A)1000	D1
Lamps	(A)1000	D2
Lamps	(A)1000	D3
Lamps	(A)1000	D4
Lamps	(A)1000	D5
Lamps	(A)1000	D6
Lamps	(A)1000	D7
Lamps	(A)1004	D0
Lamps	(A)1004	D1
Lamps	(A)1004	D2
Lamps	(A)1004	D3
Lamps	(A)1004	D4
Lamps	(A)1004	D5
Lamps	(A)1004	D6
Lamps	(A)1004	D7
Lamps	(A)1008	D0
Lamps	(A)1008	D1
Lamps	(A)1008	D2
Lamps	(A)1008	D3
Lamps	(A)1008	D4
Lamps	(A)1008	D5
Lamps	(A)1008	D6
Lamps	(A)1008	D7
Lamps	(A)100C	D0
Lamps	(A)100C	D1
Lamps	(A)100C	D2
Lamps	(A)100C	D3
Lamps	(A)100C	D4
Lamps	(A)100C	D5
Lamps	(A)100C	D6
Lamps	(A)100C	D7



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AUDIO TEST	HEX ADDRESS	DATA SWITCHES
Audio reset	(A) 6000	
Audio enable	(A) 3000	
Latch bit 0	(A) 1088	D0
Latch bit 1	(A) 1088	D1
Latch bit 2	(A) 1088	D2
Latch bit 3	(A) 1088	D3
Latch bit 0	(A) 1080	D0
Latch bit 1	(A) 1080	D1
Latch bit 2	(A) 1080	D2
Latch bit 3	(A) 1080	D3

TO END TESTING

Solder D4 pin 2 and A1 pin 1 down on PCB.  
Replace MPU in socket.

## SPRINT 1™ MEMORY MAP

### PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.

### RAM ADDRESS

0080 to 00FF

Refer to RAM test procedure.

### ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1 (L1)	006434	3000 to 33FF	3
PROM 2 (L0)	006435	3000 to 33FF	4
PROM 3 (M1)	006436	3400 to 37FF	3
PROM 4 (M0)	006437	3400 to 37FF	4
PROM 5 (N1)	006438	3800 to 3BFF	3
PROM 6 (N0)	006439	3800 to 3BFF	4
PROM 7 (P1)	006440	3C00 to 3FFF	3
PROM 8 (P0)	006441	3C00 to 3FFF	4
Track ROM 1 (D1)	006290	2000 to 27FF	1
Track ROM 2 (E1)	006290	2800 to 2FFF	1
PROGRAM ROM 3 (B1)	006442	3000 to 37FF	1
PROGRAM ROM 4 (C1)	006443	3800 to 3FFF	1

Set READ/R/W to center position, RUN/STOP to RUN, 1K/2K to 1K.

Test PROMs in pairs as indicated by brackets.

### VIDEO DISPLAY ADDRESS

(A) 0400 to 077F

Data switches 0-7

### PCB PREPARATION FOR VIDEO DISPLAY TEST

Jumper pin 37 to pin 39 on MPU socket.

Set Read R/W to R/W. Stop/Run switch to Run.

### VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

REMOVE JUMPER ON PIN 37 TO PIN 39 ON MPU SOCKET.

### PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set PCB switches on J8/9 to off. Set Read/R/W switch to Read. Game/Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Coin 1	(A)0840	D6
Coin 2	(A)0840	D7
1st gear	(A)0828	D7
2nd gear	(A)0829	D7
3rd gear	(A)082A	D7
Gas	(A)082B	D7
Start	(A)082D	D7
Self-Test	(A)082C	D7
Time 1	(A)0833	D7
Ext. play	(A)0832	D7
Coin mode 1	(A)0831	D7
Oil slicks	(A)0830	D7
Time 0	(A)0833	D6
Laps/Track change	(A)0830	D6
Coin mode 0	(A)0831	D6
Steering Dir.	(A)0880	D6
Steering Flag	(A)0880	D7

LATCH TEST	HEX ADDRESS
Timer reset	(A)0C80
Collision reset 1	(A)0D00
Steering reset 1	(A)0E00
Noise reset	(A)0F00
Attract	(A)0C00
Skid 1	(A)0C10
Start lamp 1	(A)0C30

All latches are activated  
by address switch zero.

TO END TESTING

Replace MPU in socket.

SPRINT 2™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.

RAM ADDRESS

0080 TO 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROGRAM PROM 1(L1)	006380	3000 to 33FF	3
PROGRAM PROM 2(L0)	006381	3000 to 33FF	4
PROGRAM PROM 3(M1)	006382	3400 to 37FF	3
PROGRAM PROM 4(M0)	006383	3400 to 37FF	4
PROGRAM PROM 5(N1)	006384	3800 to 3BFF	3
PROGRAM PROM 6(N0)	006385	3800 to 3BFF	4
PROGRAM PROM 7(P1)	006386	3C00 to 3FFF	3
PROGRAM PROM 8(P0)	006387	3C00 to 3FFF	4
TRACK PROM 1(F1)	006388	2000 to 23FF	3
TRACK PROM 2(F0)	006389	2000 to 23FF	4
TRACK PROM 3(H1)	006390	2400 to 27FF	3
TRACK PROM 4(H0)	006391	2400 to 27FF	4
TRACK PROM 5(J1)	006392	2800 to 2BFF	3
TRACK PROM 6(J0)	006393	2800 to 2BFF	4
TRACK PROM 7(K1)	006394	2C00 to 2FFF	3
TRACK PROM 8(K0)	006395	2C00 to 2FFF	4
TRACK ROM 1(B1)	006290	2000 to 27FF	1
TRACK ROM 2(C1)	006291	2800 to 2FFF	1
PROGRAM ROM 3(D1)	006404	3000 to 37FF	1
PROGRAM ROM 4(E1)	006405	3800 to 3FFF	1

Set READ/R/W to center position, RUN/STOP to RUN, and 1K/2K to 1K

Test Proms in pairs as indicated by brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Turn on switch 4 at location F8 on the PCB.  
Set Read R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0400 TO 077F Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

TURN OFF SWITCH 4 AT LOCATION F8 ON THE PCB.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set PCB switches on J8/9 to off. Set Read/R/W switch to Read.  
Game/Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Coin 1	(A)0840	6
Coin 2	(A)0840	7
Start 1	(A)082C	7
Start 2	(A)082D	7
Gas 1	(A)0828	7
Gas 2	(A)0829	7
1st gear, car 1	(A)0818	7
1st gear, car 2	(A)0819	7
2nd gear, car 1	(A)081A	7
2nd gear, car 2	(A)081B	7
3rd gear, car 1	(A)081C	7
3rd gear, car 2	(A)081D	7
Track Select	(A)082E	7
Self Test	(A)082A	7
Steering dir, car 1	(A)0880	6
Steering flag, car 1	(A)0880	7
Steering dir, car 2	(A)08C0	6
Steering flag, car 2	(A)08C0	7

TEST FOR SWITCHES ON PCB AT F8/9	HEX ADDRESS	DATA LED
Oil slick SW1	(A)0830	7
Track cyc SW2	(A)0830	6
Coin Mode 1 SW3	(A)0831	7
Coin Mode 0 SW4	(A)0831	6
Ext Play SW5	(A)0832	7
Spare SW6	(A)0832	6
Time 1 SW7	(A)0833	7
Time 0 SW8	(A)0833	6

DATA LATCHES	ADDRESS
Timer Reset	(A)0C80
Collision Reset 1	(A)0D00
Collision Reset 2	(A)0D80
Steering Reset 1	(A)0E00
Steering Reset 2	(A)0E80
Noise Reset	(A)0F00
Attract	(A)0C00
Skid 1	(A)0C10
Skid 2	(A)0C20
Lamp 1	(A)0C30
Lamp 2	(A)0C40

All Latches are activated  
by address switch zero.

TO END TESTING

Replace MPU in socket.

DOMINOS™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
 Jumper pin 37 to pin 39 on MPU socket.

RAM ADDRESS

0080 TO 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1 (M1)	007346	3400 to 37FF	3
PROM 2 (M0)	007347	3400 to 37FF	4
PROM 3 (N1)	007348	3800 to 3BFF	3
PROM 4 (N0)	007349	3800 to 3BFF	4
PROM 5 (P1)	007350	3C00 to 3FFF	3
PROM 6 (P0)	007351	3C00 to 3FFF	4
ROM 1 (D1)	007352	3000 to 37FF	1
ROM 2 (E1)	007438	3800 to 3FFF	1

Set READ/R/W to center position, RUN/STOP to RUN, and 1K/2K to 1K.  
  
 Test PROMs in pairs as indicated in brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read/R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0400-07FF Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

REMOVE JUMPER FROM PIN 37 TO PIN 39 ON MPU SOCKET.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read/R/W switch to Read. Game/Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Coin 1	(A)0840	D6
Coin 2	(A)0840	D7
1 up	(A)0818	D7
1 rt	(A)0819	D7
1 down	(A)081A	D7
1 left	(A)081B	D7

SWITCH TEST, cont.

	HEX ADDRESS	DATA LED
2 up	(A)0828	D7
2 rt	(A)0829	D7
2 down	(A)082A	D7
2 left	(A)082B	D7
Start 1	(A)082C	D7
Start 2	(A)082D	D7
Self-test	(A)082E	D7
\$ Mode 0	(A)0831	D6
\$ Mode 1	(A)0831	D7
Heat Option 0	(A)0830	D6
Heat Option 1	(A)0830	D7

LATCH TEST

	HEX ADDRESS
Timer reset	(A)0C80
Attract	(A)0C00
Tumble	(A)0C10
Lamp 1	(A)0C30
Lamp 2	(A)0C40

All latches are activated  
by address switch zero.

TO END TESTING

Replace MPU in socket.

4-PLAYER DOMINOS™ (COCKTAIL TABLE) MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
 Jumper pin 37 to 39 on MPU socket.

RAM ADDRESS

0080 to 00FF

Refer to RAM test procedure.

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1 (L1)	007754	3000 to 33FF	3
PROM 2 (L0)	007755	3000 to 33FF	4
PROM 3 (M1)	007756	3400 to 37FF	3
PROM 4 (M0)	007757	3400 to 37FF	4
PROM 5 (N1)	007758	3800 to 3BFF	3
PROM 6 (N0)	007759	3800 to 3BFF	4
PROM 7 (P1)	007760	3C00 to 3FFF	3
PROM 8 (P0)	007761	3C00 to 3FFF	4
ROM 1 (O1)	007762	3000 to 37FF	1
ROM 2 (E1)	007763	3800 to 3FFF	1

Set READ/R/W to center position, RUN/STOP to RUN, and 1K/2K to 1K.

Test PROMs in pairs as indicated by brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0400-07FF Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

REMOVE JUMPER FROM PIN 37 TO PIN 39 ON MPU SOCKET.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W switch to Read. Game Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
1 start	(A)081A	D7
1 up	(A)0818	D7
1 rt	(A)0819	D7
1 down	(A)081A	D7
1 left	(A)081B	D7
2 up	(A)081C	D7
2 rt	(A)081D	D7





## NIGHT DRIVER™ MEMORY MAP

### PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.

### RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

### ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1 (H1)	006560	9000 to 93FF	3
PROM 2 (C1)	006561	9000 to 93FF	4
PROM 3 (J1)	006562	9400 to 97FF	3
PROM 4 (D1)	006563	9400 to 97FF	4
PROM 5 (K1)	006564	9800 to 9BFF	3
PROM 6 (E1)	006565	9800 to 9BFF	4
PROM 7 (L1)	006566	9CFF to 9FFF	3
PROM 8 (F1)	006567	9CFF to 9FFF	4
ROM 1 (D2)	006569	9000 to 97FF	1
ROM 2 (F2)	006570	9800 to 9FFF	1

Set READ/R/W to center position, STOP/RUN to RUN and 1K/2K to 1K

Test PROMs two at a time as indicated by brackets.

### PCB PREPARATION FOR VIDEO DISPLAY TEST

Jumper pin 37 to pin 39 on MPU socket.  
Set Read R/W to R/W. Stop/Run switch to Run.

### VIDEO DISPLAY ADDRESS

(A) 0200-03FF. Data switches 0-7.

### VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

TAKE JUMPER OFF PIN 37 TO PIN 39 ON MPU SOCKET.

### PCB PREPARATION FOR SWITCH AND LATCH TESTS

Read R/W switch set to Read. Game Box switch set to Game.

SWITCH AND LATCH TEST	HEX ADDRESS	DATA LED
Coin 1	(A) 0800	D7
Coin 2	(A) 0801	D7
Start	(A) 0802	D7
Acc	(A) 0803	D7
Expert	(A) 0804	D7
Novice	(A) 0805	D7
Line Fri Lamp	(A) 0806	D7
50Z	(A) 0807	D7

SWITCH AND LATCH TEST,cont.	HEX ADDRESS	DATA LED
OPT 0-4	(A) 0600	D4-7
Track Set	(A) 0601	D4
Bonus Time	(A) 0601	D5
V Blank	(A) 0601	D6
Test	(A) 0601	D7
Gear 1	(A) 0602	D4
Gear 2	(A) 0602	D5
Gear 3	(A) 0602	D6
Difficult Bonus	(A) 0603	D5
Steer A	(A) 0603	D6
Steer B	(A) 0603	D7

LATCH TEST	HEX ADDRESS	DATA SWITCHES
Speed 1	(A) 0A00	D0
Speed 2	(A) 0A00	D1
Speed 3	(A) 0A00	D2
Speed 4	(A) 0A00	D3
Skid 1	(A) 0A00	D4
Skid 2	(A) 0A00	D5
Crash	(A) 0C00	D0
Attract	(A) 0C00	D1
Spare	(A) 0C00	D2
Not used	(A) 0C00	D3
Led start	(A) 0C00	D4

TO END TESTING

Replace MPU in socket.

CANYON BOMBER™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.

RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1(L1)	009497	3000 to 33FF	3
PROM 2(K1)	009498	3000 to 33FF	4
PROM 3(J1)	009499	3400 to 37FF	3
PROM 4(H1)	009500	3400 to 37FF	4
PROM 5(M1)	009501	3800 to 3BFF	3
PROM 6(N1)	009502	3800 to 3BFF	4
PROM 7(P1)	009503	3C00 to 3FFF	3
PROM 8(R1)	009504	3C00 to 3FFF	4
ROM 1 (F1)	009493	2000 to 27FF	1
ROM 2 (B1)	009494	2800 to 2FFF	1
ROM 3 (C1)	009495	3000 to 37FF	1
ROM 4 (D1)	009496	3800 to 3FFF	1

Set READ/R/W to center position, STOP/RUN to RUN, and 1K/2K to 1K.

Test PROMs two at a time as indicated by brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Jumper pin 37 to pin 39 on MPU socket.  
Set Read R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0900-0BBF Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

REMOVE JUMPER FROM PIN 37 TO PIN 39 ON MPU SOCKET.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W switch to Read. Game Box switch to Game.

SWITCH AND LATCH TEST	HEX ADDRESS	DATA LED
Coin 1	(A)1000	D7
Coin 2	(A)1001	D7
Start 1	(A)1002	D7
Start 2	(A)1003	D7
Test SW	(A)1004	D7
V Blank	(A)1005	D7
H Score Rst	(A)1006	D7
Slam SW	(A)1007	D7
Fire 1	(A)1002	D0
Fire 2	(A)1003	D0
OPTIONS TEST	HEX ADDRESS	DATA LED
Switch 1	(A)1803	D0
Switch 2	(A)1803	D1
Switch 3	(A)1802	D0
Switch 4	(A)1802	D1
Switch 5	(A)1801	D0
Switch 6	(A)1801	D1
Switch 7	(A)1800	D0
Switch 8	(A)1800	D1
LATCHES TEST	HEX ADDRESS	
Whistle 1	(A)0600	
Whistle 2	(A)0601	
Lamp 1	(A)0680	All Latches are activated by address switch 1.
Lamp 2	(A)0681	
Attract 1	(A)0700	
Attract 2	(A)0701	
AUDIO TEST	HEX ADDRESS	
Motor 1	(A)0400	
Motor 2	(A)0401	Data switches 0-3 will operate latches.
Explosion	(A)0500	
Watch Dog	(A)0501	

TO END TESTING

Replace MPU in socket.

SUPER BUG MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.

RAM TEST PCB PREPARATION

Short F4, pin 13, to ground.

RAM ADDRESS

0000-00FF

To end RAM TEST, remove short between F4, pin 13 and ground.

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1 (E2)	009115	0800 to 0BFF	3
PROM 2 (H2)	009116	0800 to 0BFF	4
PROM 3 (K2)	009117	0C00 to 0FFF	3
PROM 4 (E1)	009118	0C00 to 0FFF	4
PROM 5 (H1)	009119	1000 to 13FF	3
PROM 6 (K1)	009120	1000 to 13FF	4
PROM 7 (F2)	009462	1400 to 17FF	3
PROM 8 (J2)	009463	1400 to 17FF	4
PROM 9 (L2)	009464	1800 to 1BFF	3
PROM 10 (F1)	009465	1800 to 1BFF	4
PROM 11 (J1)	009466	1C00 to 1FFF	3
PROM 12 (L1)	009467	1C00 to 1FFF	4
ROM 1 (D1)	009121	0800 to 0FFF	1
ROM 2 (C1)	009122	1000 to 17FF	1
ROM 3 (A1)	009123	1800 to 1FFF	1

Set READ/R/W to center position, STOP/RUN to RUN and 1K/2K to 1K.

Test Proms in pairs as indicated by brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read/R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

- (A) 0400-047F: Alpha-numeric Display - Data switches 0-7
- (A) 0800-08FF: Playfield Display - Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read/R/W switch to Read. Game/Box switch to Game.

SWITCH AND LATCH TEST	HEX ADDRESS	DATA LED
Coin 1	(A) 0203	7
Coin 2	(A) 0204	7
Start	(A) 0205	7
1st Gear	(A) 0201	7
2nd Gear	(A) 0200	0
3rd Gear	(A) 0200	7

SWITCH AND LATCH TEST, cont.	HEX ADDRESS	DATA LED
Slam Sw.	(A) 0207	0
Track Sel	(A) 0207	7
Skid in	(A) 0206	0
Hi Score Rst	(A) 0203	0
Test	(A) 0205	0
Gas	(A) 0201	0
Str Flag	(A) 0202	7
Str Dir	(A) 0202	0
Crash in	(A) 0206	7

PCB SWITCH TEST	HEX ADDRESS	DATA LED
SW1	(A) 0283	0
SW2	(A) 0283	1
SW3	(A) 0282	0
SW4	(A) 0282	1
SW5	(A) 0281	0
SW6	(A) 0281	1
SW7	(A) 0280	0
SW8	(A) 0280	1

LATCH TEST	HEX ADDRESS	
Motor Sound	(A) 0280	0-3
Crash Sound	(A) 02A0	4-7
Skid Sound	(A) 02C0	N/A
Skid Reset	(A) 0160	N/A
PVP load	(A) 0100	0-7
PHP load	(A) 0120	0-7
Crash Reset	(A) 0140	N/A
Car Rot	(A) 0180	0-5
Steering Rst	(A) 01A0	N/A
Watch Dog	(A) 01C0	N/A
Arrow Off	(A) 01E0	N/A

DESTROYER™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Cut and lift B2 pin 8 on PCB.

RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 0 (E2)	030141	7800 to 7BFF	3
PROM 1 (F3)	030142	7800 to 7BFF	4
PROM 2 (H2)	030143	7C00 to 7FFF	3
PROM 3 (J3)	030144	7C00 to 7FFF	4
ROM 1 (C3)	030145	7800 to 7FFF	1

Set READ/R/W to center position, STOP/RUN to RUN, and 1K/2K to 1K

PCB PREPARATION FOR VIDEO DISPLAY TEST

Resolder B2 pin 8 back down on PCB.  
Set Read R/W to R/W. Stop/Run switch to Run.

Test Proms two at a time as indicated by brackets.

VIDEO DISPLAY ADDRESS

(A) 3000 to 30FF Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W switch to Read. Game Box switch to Game.

SWITCH AND LATCH TEST

SWITCHES TEST	HEX ADDRESS	DATA
Coin 1	(A) 1001	4
Coin 2	(A) 1001	5
Start 1	(A) 1000	4
Start 2	(A) 1000	5



SWITCHES TEST, cont.	HEX ADDRESS	DATA LEDs
Extended play 1	(A)1000	7
Extended play 0	(A)1000	6
V Blank	(A)1001	7
Test	(A)1001	3
Rlse	(A)1001	2
Slow	(A)1001	1
Slam	(A)1001	0
Potsense 2	(A)1000	3
Potsense 1	(A)1000	2

PCB SWITCH TEST	HEX ADDRESS	DATA LEDs
Credit Mode 0	(A)2000	0
Credit Mode 1	(A)2000	1
Game Time 0	(A)2000	2
Game Time 1	(A)2000	3
Language 0	(A)2000	4
Language 1	(A)2000	5

LATCHES TEST	HEX ADDRESS
Credit Lamp 1	(A)1000
Credit Lamp 2	(A)1001
Son Gate	(A)1002
Launch	(A)1003
Explosion	(A)1004
Sonar	(A)1005
High Explosion	(A)1006
Low Explosion	(A)1007

All latches are activated  
by DATA switch zero.

MISC. TEST	HEX ADDRESS	DATA
Major Object Attributes	(A)4000	0-3
Major Object H Pos	(A)4000	0-7
Cursor Load/Watch Dog	(A)5000	0-7
Interrupt Acknowledge	(A)5001	N/A
Picture 0 Load	(A)5002	0-3
Picture 1 Load	(A)5003	0-3
H Position 0 Load	(A)5004	0-7
H Position 1 Load	(A)5005	0-7
V Position 0 Load	(A)5006	0-7
V Position 1 Load	(A)5007	0-7

TO END TESTING

Replace MPU in socket.

DRAG RACE™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Lift H3 pin 6 off PCB.

RAM ADDRESS

0080 to 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
ROM 1 (C1)	008513	1000 to 17FF	1
ROM 2 (A1)	008514	1800 to 1FFF	1

Set READ/R/W to center position and RUN/STOP to RUN.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read/R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0A00 to 0AFF Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

SOLDER H3 PIN 6 DOWN ON PCB.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W/switch to Read. Game/Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Coin SW1	(A)0810	7
Coin SW2	(A)0818	7
1 player start	(A)0820	7
2 player start	(A)0828	7
Game price SW5	(A)0830	7
Game price SW6	(A)0838	7



STARSHIP 1™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test  
Short B5 pin 15 to ground

RAM ADDRESS

0000 to 03FF

Refer to RAM test procedure

ROM ADDRESS

PROM 1 (C/D1)	007528	2C00 to 2FFF	3
PROM 2 (C/D2)	007529	2C00 to 2FFF	4
PROM 3 (H1)	007520	3000 to 33FF	3
PROM 4 (H2)	007521	3000 to 33FF	4
PROM 5 (F1)	007522	3400 to 37FF	3
PROM 6 (F2)	007523	3400 to 37FF	4
PROM 7 (E/F1)	007524	3800 to 3BFF	3
PROM 8 (E/F2)	007525	3800 to 3BFF	4
PROM 9 (D/E1)	007526	3C00 to 3FFF	3
PROM 10 (D/E2)	007527	3C00 to 3FFF	4
ROM A (H3)	007530	3000 to 37FF	1
ROM B (E3)	007531	3800 to 3FFF	1

Set READ/R/W to center position, RUN/STOP to RUN, and 1K/2K to 1K.

Test PROMs in pairs as indicated by brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read R/W to R/W. Stop/Run switch to Run. Ground N10 pin 3.

VIDEO DISPLAY ADDRESS

(A) C800 to C9FF Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

NOW REMOVE SHORT FROM B5 PIN 15 and N10 PIN 3.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W switch to Read. Game Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Phasor	(A)A000	D0
Spare	(A)A000	D1
Photon Torpedo	(A)A000	D2
Start	(A)A000	D3
Coin	(A)A000	D4
Spare	(A)A000	D5
Slow	(A)A000	D6
Coin	(A)A000	D7

LATCH TEST	HEX ADDRESS	DATA SWITCH
Noise Freq.	(A)DE06	D0
Molvl	(A)DE05	D0
Sl 2	(A)DE04	D0
Sl 1	(A)DE03	D0
Kicker	(A)DE02	D0
Phasor On	(A)DE01	D0
Attract	(A)DE00	D0
Pitch Pot (input)	(A)DD00	
Roll Pot (input)	(A)DD01	
Speed Pot (input)	(A)DD02	
Game Time (input)	(A)DD03	

MISC. TEST	HEX ADDRESS	DATA SWITCH
Ship Explode	(A)DC00	D0
Circle Mod	(A)DC01	D0
Circle Kill	(A)DC02	D0
Starfield Kill	(A)DC03	D0
Hyperspace	(A)DC04	D0
Blackhole	(A)DC05	D0
Mux	(A)DC06	D0
Spare	(A)DC07	D0

ANALOG OUT TEST	HEX ADDRESS	DATA SWITCHES
Spare	(A)DF00	D0-7
Spaceship size	(A)DF01	D0-7
Noise Amplitude	(A)DF02	D0-7
Tone Pitch	(A)DF03	D0-7
Motor Speed	(A)DF04	D0-7
H Pos circle	(A)DF05	D0-7
V Pos circle	(A)DF06	D0-7
Size circle	(A)DF07	D0-7

COLLISION LATCH TEST	HEX ADDRESS	DATA SWITCHES
Circle visible	(A)C400	D0
Circle & Bullet	(A)C400	D1
Bullet & Ship	(A)C400	D2
Spare	(A)C400	D3
Extended Play	(A)C400	D4-7

MISC. TEST

H Pos. (16 objects)	(A)CC0X	D0-7
V Pos. (16 objects)	(A)D00X	D0-7
Graphics Select	(A)D40X	D0-2
Graphics Briteness	(A)D40X	D3
Space Ship picture	(A)C300-C3FF	D0-2
Space Ship Left/Right	(A)C300-C3FF	D7

TO END TESTING

Replace MPU in socket.

ULTRA TANK™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.  
Cut and lift C4 pin 3, B4 pin 12.

RAM ADDRESS

0000 to 00FF

Refer to RAM test procedure

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET	
PROM 3 (N1)	030180	B000 to B7FF	3	Set READ/R/W to center position, RUN/STOP to RUN, and 1K/2K to 2K.
PROM 3 (K1)	030181	B000 to B7FF	4	
PROM 4 (M1)	030182	B800 to BFFF	3	
PROM 4 (L1)	030183	B800 to BFFF	4	
ROM 3 (D1)	030178	B000 to B7FF	1	Test PROMS in pairs as indicated by brackets.
ROM 4 (E1)	030179	B800 to BFFF	1	

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read/R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0800 to 0BFF. Data switch 0-7.

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

Solder down C4 pin 3, B4 pin 12.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W switch to Read. Game Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Start 1	(A) 2000	D7
Joy W	(A) 2001	D7
Start 2	(A) 2002	D7
Joy Y	(A) 2003	D7
Fire A	(A) 2004	D7
Joy X	(A) 2005	D7
Fire B	(A) 2006	D7
Joy Z	(A) 2007	D7

SWITCH TEST, cont.	HEX ADDRESS	DATA LED
Coin 1	(A) 2020	D7
Coin 2	(A) 2022	D7
Invisible	(A) 2024	D7
Rebound	(A) 2026	D7
Barrier Read	(A) 1800	D7
Test	(A) 1000	D6
V Blank	(A) 1000	D7
Lang 0	(A) 2060	D0
Lang 1	(A) 2060	D1
Credit 0	(A) 2061	D0
Credit 1	(A) 2061	D1
Time 0	(A) 2062	D0
Time 1	(A) 2062	D1
Spare	(A) 2063	D0
Spare	(A) 2063	D1
Collision Read	(A) 204X	D7
Slam	(A) 2046	D7
Collision 1 Reset	(A) 2020	D7
Collision 2 Reset	(A) 2022	D7
Collision 3 Reset	(A) 2024	D7
Collision 4 Reset	(A) 2026	D7
Write D/A latch	(A) 2040	D7
Write Explosion	(A) 2042	D7
Timer Reset	(A) 2044	D7

LATCH TEST

HEX ADDRESS

Fire 1	(A) 206E
Fire 2	(A) 206C
Led 2	(A) 206A
Led 1	(A) 2068
Lockout	(A) 2066

All latches are activated  
by data switch zero.

TO END TESTING

Replace MPU in socket.



TRIPLE HUNT™ MEMORY MAP

PCB PREPARATION FOR ALL TESTS

Remove MPU from PCB under test.

RAM ADDRESS

0000 to 00FF

NOTE: Before performing RAM test, cut and lift D6 pin 10. When completed with RAM test, solder D6 pin 10 back down.

Refer to RAM test procedure.

ROM ADDRESS

ROM#	PART #	ADDRESS	SOCKET
PROM 1 (C/D2)	008405	1000 to 13FF	3
PROM 2 (C/D1)	008401	1000 to 13FF	4
PROM 3 (D2)	008406	1400 to 17FF	3
PROM 4 (D1)	008402	1400 to 17FF	4
PROM 5 (E2)	008407	1800 to 1BFF	3
PROM 6 (E1)	008403	1800 to 1BFF	4
PROM 7 (F2)	008408	1C00 to 1FFF	3
PROM 8 (F1)	008404	1C00 to 1FFF	4
ROM 1 (J1)	008791	1000 to 17FF	1
ROM 2 (H1)	008790	1800 to 1FFF	1

Set READ/R/W to center position, RUN/STOP to RUN and 1K/2K to 1K.

Test PROMs in pairs as indicated by brackets.

PCB PREPARATION FOR VIDEO DISPLAY TEST

Set Read R/W to R/W. Stop/Run switch to Run.

VIDEO DISPLAY ADDRESS

(A) 0400 to 07FF. Data switches 0-7

VIDEO DISPLAY SPECIAL INSTRUCTIONS

Start with all data switches set at zero. Count in binary with the data switches. Each switch setting will change the characters displayed on the screen. Press the reset button on the RAM/ROM tester to initiate the display.

Solder D6 pin 9 back on the PCB.

PCB PREPARATION FOR SWITCH AND LATCH TESTS

Set Read R/W switch to Read. Game Box switch to Game.

SWITCH TEST	HEX ADDRESS	DATA LED
Test	(A) 0C48	D6
Slam	(A) 0C40	D6
Coin mode 0	(A) 0C0A	D6
Game bit 0	(A) 0C09	D6
Time 0	(A) 0C08	D6
Start	(A) 0C00	D6
Trigger	(A) 0C48	D7
Coin switch 2	(A) 0C40	D7
Ext. play	(A) 0C0B	D7

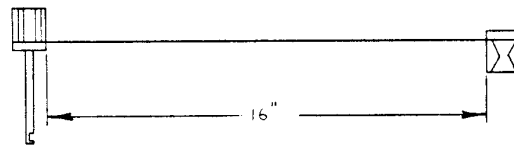
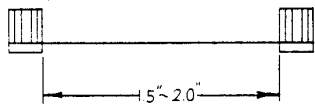
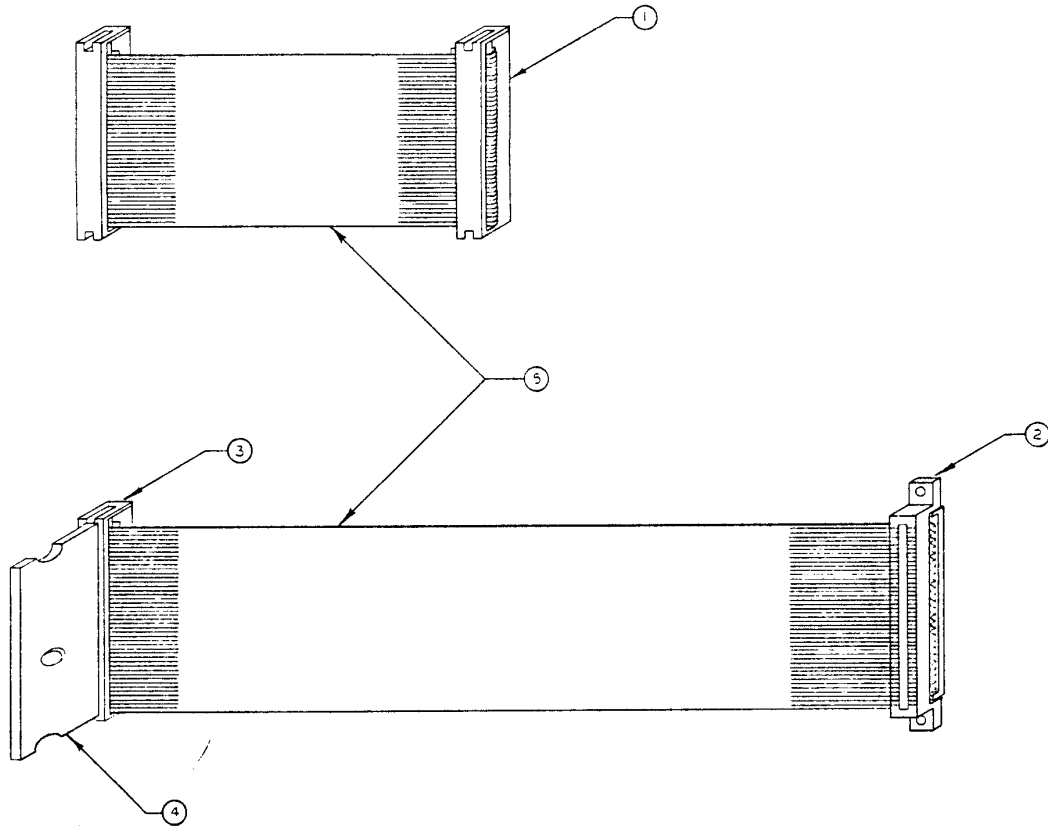
SWITCH TEST, cont.	HEX ADDRESS	DATA LED
Coin mode 1	(A) 0C0A	D7
Game bit 1	(A) 0C09	D7
Time 1	(A) 0C08	D7
Coin switch 1	(A) 0C00	D7
LATCH TEST	HEX ADDRESS	
Window	(A) 0C38	
Lamp 1	(A) 0C32	
Coin lockout	(A) 0C36	All latches are activated by data switch zero.
Screech	(A) 0C34	
RAM 2	(A) 0CA0	
Tape control	(A) 0CA2	
Bear	(A) 0CA4	
MISC. TEST	HEX ADDRESS	DATA
U Motion W	(A) 0800	D0-7
H Motion W	(A) 0810	D0-7
Organ RAM W	(A) 0820	D0-7
Object Code		
RAM write	(A) 0830	D0-3
IO	(A) 0C00	D6-7
D-A latch	(A) 0C10	D0-3
Cram	(A) 0C20	D1-4
1ø3	(A) 0C30	D0-3,D7

TO END TESTING

Replace MPU in socket.

E. ROM/RAM TESTER SUPPORT DOCUMENTS

Including ROM/RAM PCB Assemblies, Schematics, and Parts List.

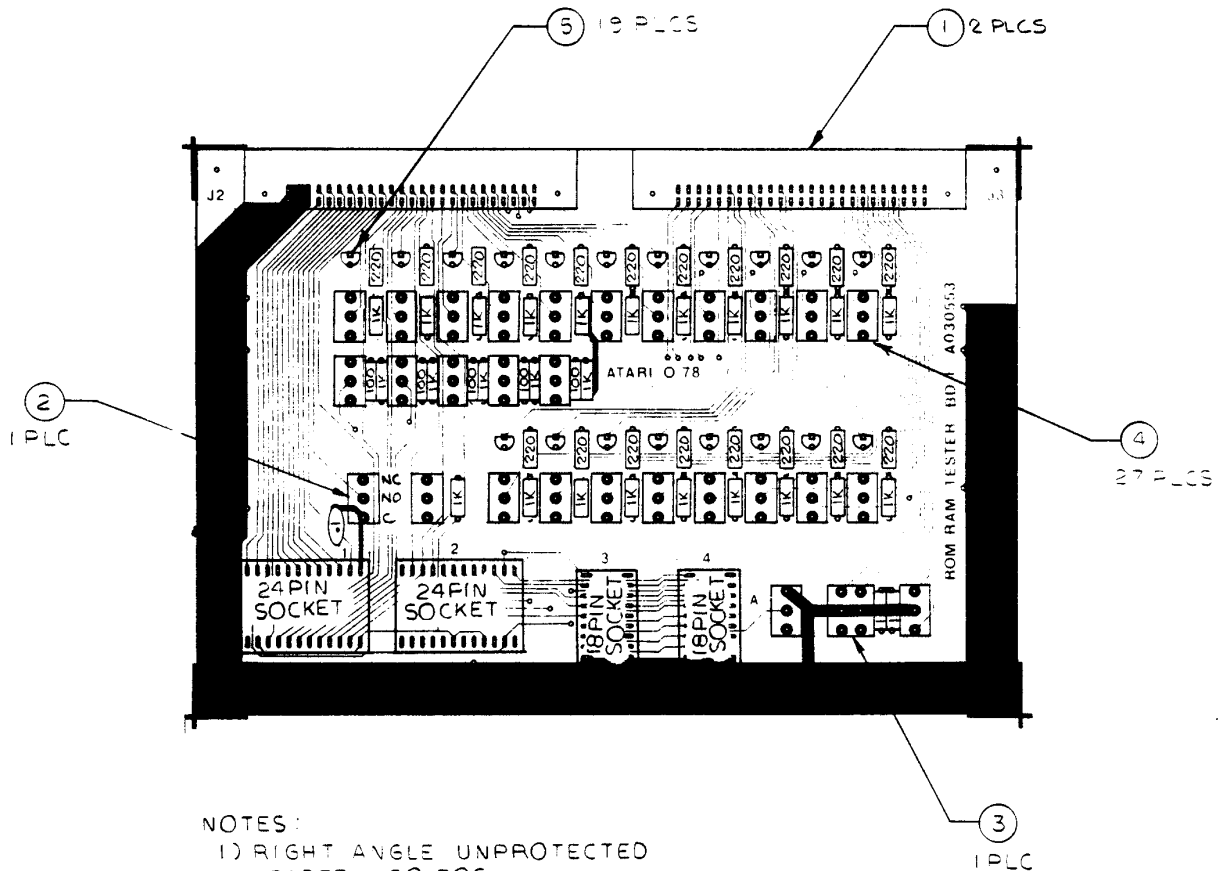


NOTES

- 1) T & B / ANSLEY  
P/N 609-5001 M
- 2) T & B / ANSLEY  
P/N 609-5005 M  
WITH MOUNTING EARS
- 3) T & B / ANSLEY  
P/N 609-5006 (SOCKET)
- 4) EXTRACTOR HANDLE  
P/N 609-5031
- 5) FLAT CABLE P/N 171-50  
MFG T & B / ANSLEY

Tester Cable Assembly Drawing  
A030552-01





NOTES:

- 1) RIGHT ANGLE UNPROTECTED  
HEADER 50 POS.
- 2) MOMENTARY PUSH BUTTON SW.
- 3) TOGGLE SW. DPDT
- 4) TOGGLE SW. SPDT
- 5) LED P/N 38-ME 7124

PCB #1 Assembly Drawing  
A030553-01



ITEM	DESCRIPTION	MFR. PART NO. ATARI DWG NO.	QTY
1	Rt. Angle Header (Unprotected)	<u>801-067</u> Spectra-Strip	5
	Female Socket Transition Connector (With Strain Relief)	<u>609-5001M</u> T&B/Ansley	4
3	Female Socket Transition Connector (Without Strain Relief)	<u>609-5000M</u> T&B/Ansley	1
4	Extractor Handle For P/N 609-5000M	<u>609-5031SP</u> T&B/Ansley	1
5	Card Edge Connector With Full Mounting Ears	<u>609-5005M</u> T&B/Ansley	1
6	Series 171, 28 AWG Stranded Round Conductor Flat Cable	<u>171-50</u> T&B/Ansley	17"
7	Toggle Switch SPDT	<u>7101-SD-CB-E</u> C&K Comp. Inc.	29
8	Toggle Switch DPDT	<u>7203-SD-CB-E</u> C&K Comp. Inc.	1
9	Momentary Push Button Switch With Dress Nut (P/N8025)	<u>8125-C-E</u> C&K Comp. Inc.	1
10	Cap (Medium Red)	<u>8018-3</u> C&K Comp. Inc.	1
11	Spacer Clearance Hole Class 10 1/2" Nylon	<u>10R-4-06-8N</u> Positronic Ind.	4
12	S.A.E. Socket 24 Pin	<u>MB-153900-24E</u> 79-42024	2
13	S.A.E. Socket 19 Pin	<u>MB-153901-18E</u> 79-42018	2
14	L.E.D. Atari P/N	<u>1</u> <del>78-my-o13</del>	19
15	1k ohm 1/4 W Resistor Atari P/N	<u>10-5102</u>	33
16	220 ohm 1/4 W. Resistor Atari P/N	<u>10-5221</u>	19
17	100 ohm 1/4 W. Resistor Atari P/N	<u>10-5101</u>	5
18	47k ohm 1/4 W. Resistor Atari P/N	<u>10-5473</u>	2
19	18k ohm 1/4 W. Atari P/N	<u>10-5183</u>	1
20	100 uf Tantalum Atari P/N	<u>29-001</u>	1









ITEM	DESCRIPTION	MFR. PART NO. ATARI DWG NO.	QTY
21	.022 uf (disc) Atari P/N	<u>27-250223</u>	1
22	2.2uf (Tantalum) Atari P/N	<u>29-010</u>	1
23	220 pf Cap Atari P/N	<u>28-101221</u>	1
24	0.01uf (Disc) Atari P/N	<u>27-250103</u>	1
25	1N914 (Diodes) Atari P/N	<u>31-1N914</u>	1
26	By Pass Caps (0.1uf Disc) Atari P/N	<u>29-005</u>	7
27	I.C. 9316 Atari P/N	<u>37-9316</u>	3
28	I.C. 7404 Atari P/N	<u>37-7404</u>	4
29	I.C. .555 Atari P/N	<u>37-555</u>	1
0	I.C. 7474 Atari P/N	<u>37-7474</u>	1
31	I.C. 74367 (8T97) Atari P/N	<u>37-74367</u>	6
32	I.C. 7408 Atari P/N	<u>37-7408</u>	1
33	I.C. 7410 Atari P/N	<u>37-7410</u>	1
34	I.C. 9602 Atari P/N	<u>37-9602</u>	1
35	I.C. 7427 Atari P/N	<u>37-7427</u>	1
36	I.C. 7486 Atari P/N	<u>37-7486</u>	2
37	Rubber Feet (Sticker Type)	<u>5003</u> 3M & Co.	4
38	Sheet Metal Screw 6-32 Size		4
39	Machine Screws 6 - 32 x 3/4"		4
40	Enclosure (RAM-ROM Auto Box)		1

